AMT49700

Automotive Stepper Driver

FEATURES AND BENEFITS

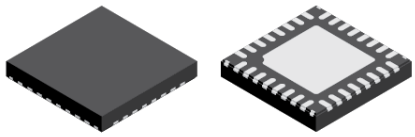
- Peak motor current up to 1.6 A at 28 V.
- Low $R_{DS(ON)}$ outputs, 0.5 Ω source and sink typical
- Continuous operation at high ambient temperature
- 3.7 to 42 V supply operation
- Adaptive mixed current decay
- Synchronous rectification for low power dissipation
- Output slew control and PWM frequency spreading for EMC noise reduction
- Internal overvoltage and undervoltage lockout
- Hot warning and overtemperature shutdown
- Short-circuit, open-load diagnostics
- Programmable motion control
- Configurable through serial interface
- Simple step and direction control option

APPLICATIONS

- Automotive stepper motors
- Engine management
- Headlamp positioning
- HVAC flap and valve control

PACKAGE:

32-Pin QFN with Exposed Thermal Pad (suffix ET)



Not to scale

DESCRIPTION

The AMT49700 is a flexible microstepping stepper motor driver with integrated phase current control, a built in translator, and simple motion control. It is a single chip solution designed to operate bipolar stepper motors in full, half, quarter, eighth and sixteenth step modes, at up to 28 V.

The current regulator operates with fixed frequency PWM and uses adaptive mixed current decay to reduce audible motor noise and increase step accuracy. The current in each phase of the motor is controlled through a DMOS full-bridge using synchronous rectification to improve power dissipation. Internal circuits and timers prevent cross-conduction and shoot through when switching between high-side and low-side drives.

The outputs are protected from short circuits and features for low load current detection are included. Chip level protection includes hot thermal warning, overtemperature shutdown, overvoltage lockout, and undervoltage lockout.

The AMT49700 is fully controlled and configured through an SPI-compatible serial interface. It provides single step control with adjustable microstep resolution for fine positioning control and programmable motion control providing independent motor acceleration, deceleration, start speed, run speed, and number of steps with a single SPI command. In addition, detailed diagnostics are available on the serial data output.

The AMT49700 is supplied in a 32-terminal 5 mm × 5 mm QFN package with an exposed thermal pad (package type ET).

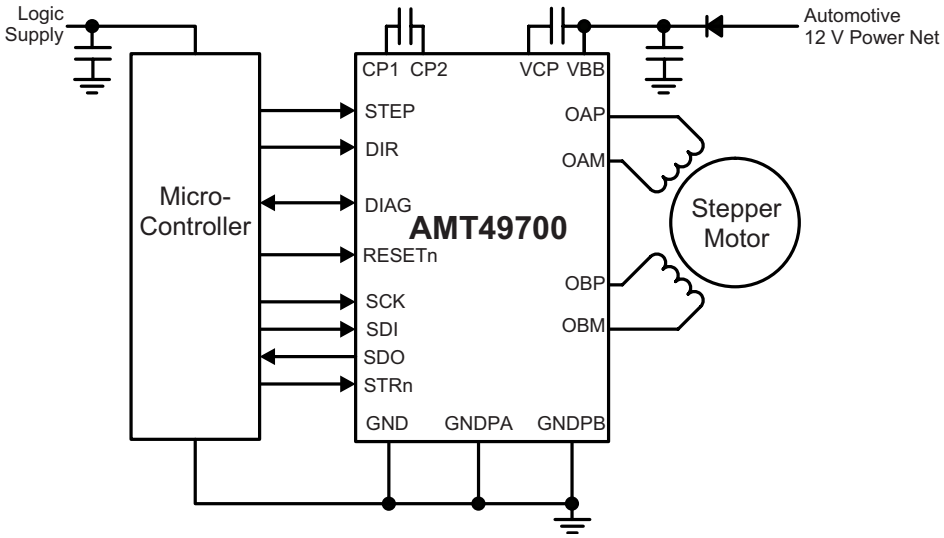


Figure 1: Typical Application Diagram

Selection Guide

Part Number	Packing	Package
AMT49700KETJTR	1500 pieces per 7-inch reel	5 mm × 5 mm, 0.9 mm nominal height QFN with exposed thermal pad

Table of Contents

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		–0.3 to 42	V
Terminal CP1	V_{CP1}		–0.3 to V_{BB} + 0.3	V
Terminal CP2	V_{CP2}		–0.3 to V_{BB} + 8	V
Terminal VCP	V_{CP}		–0.3 to V_{BB} + 8	V
Terminals STEP, DIR, SCK, SDI, SDO, STRn			–0.3 to 6	V
Terminal RESETn	V_{RESETn}	Can be pulled to V_{BB} with 33 kΩ	–0.3 to 6	V
Terminal DIAG	V_{DIAG}		–0.3 to 40	V
Terminals OAP, OAM, OBP, OBM			–0.3 to V_{BB}	V
Terminals GNDPA, GNDPB	V_{GNDPA}, V_{GNDPA}	All ground terminals must be connected together	–0.1 to 0.1	V
Ambient Operating Temperature Range [2]	T_A		–40 to 150	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		165	°C
Transient Junction Temperature	T_{Jt}	Overtemperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, ensured by design and characterization.	175	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[1] With respect to GND
[2] Limited by power dissipation

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	High-K PCB (multilayer with significant copper areas, based on JEDEC standard JESD51-7)	30	°C/W

[3] Additional thermal information available on the Allegro website.

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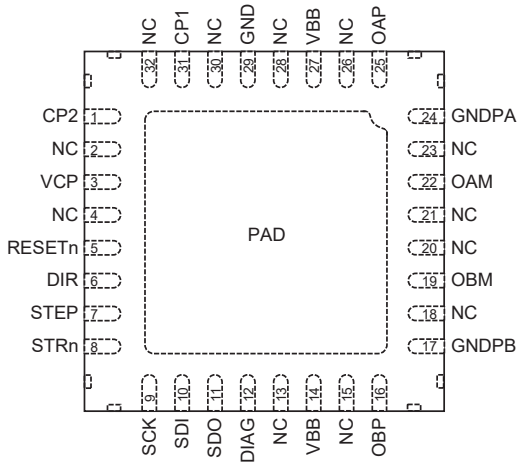
PINOUT DIAGRAM AND TERMINAL LIST



Package ET, 32-Pin eQFN Pinout Diagram

Terminal List Table

Number	Name	Function
31	CP1	Charge Pump Capacitor
1	CP2	Charge Pump Capacitor
12	DIAG	Diagnostic output
6	DIR	Direction Input
29	GND	Ground
24	GNDPA	Power Ground for A Phase
17	GNDPB	Power Ground for B Phase
22	OAM	Bridge A negative output
25	OAP	Bridge A positive output
19	OBM	Bridge B negative output
16	OBP	Bridge B positive output
5	RESETn	Standby Mode Control
9	SCK	Serial Clock Input
10	SDI	Serial Data Input
11	SDO	Serial Data Output
7	STEP	Step Input
8	STRn	Serial Strobe (chip select) Input
27	VBB	Main Supply
14	VBB	Main Supply
3	VCP	Pump Storage Capacitor
PAD	–	Exposed Thermal Pad

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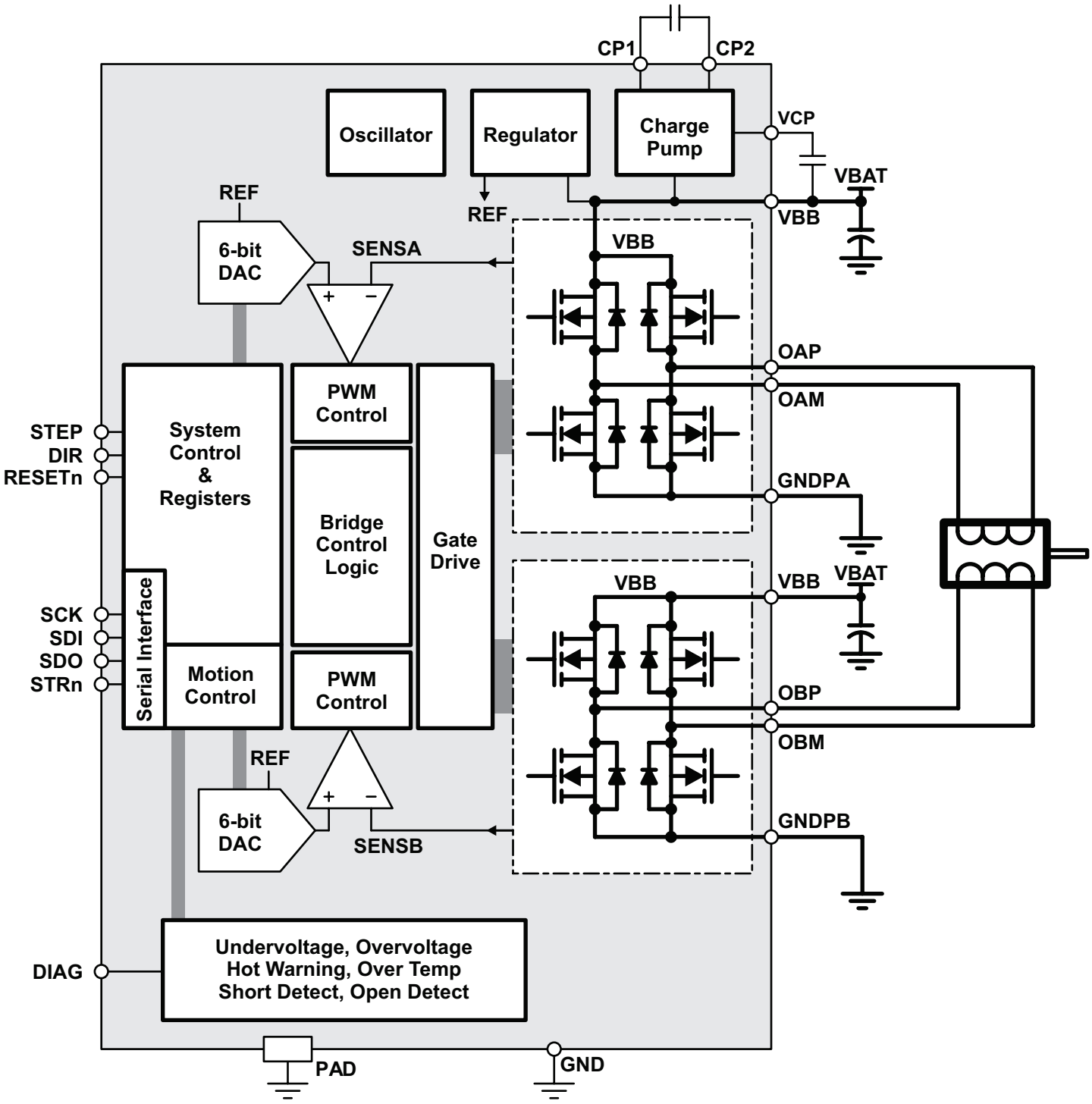
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 28 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
SUPPLIES						
Supply Voltage Range [4][5]	V_{BB}	No unsafe states	0	–	42	V
		Outputs driving	5.5	–	V_{BBOV}	V
Supply Quiescent Current	I_{BBQ}	DIS = 1	–	–	25	mA
		Sleep Mode, V_{BB} = 12 V, GTS = 1, STRn = 1 or V_{RESETn} < 0.5 V, T_J = 25°C	–	20	40	µA
		Sleep Mode, V_{BB} = 12 V, GTS = 1, STRn = 1 or V_{RESETn} < 0.5 V, T_J = 150°C	–	60	100	µA
Logic I/O Regulator Voltage	V_{LIO}	VLR = 0	3.1	3.3	3.5	V
		VLR = 1	4.8	5.0	5.2	V
Charge Pump Voltage	V_{CP}	With respect to V_{BB}, V_{BB} > 7.5 V, DIS = 1, GTS = 0, RESETn = 1	–	7.0	–	V
MOTOR BRIDGE OUTPUT						
High-Side On-Resistance	R_{ONH}	V_{BB} ≥ 7 V, I_{OUT} = –1 A [1], T_J = 25°C	–	500	600	mΩ
		V_{BB} = 13.5 V, I_{OUT} = –1 A [1], T_J = 150°C	–	900	1100	mΩ
High-Side Body Diode Forward Voltage	V_{FH}	I_F = 1 A	–	–	1.4	V
		I_F = 0.1 A	–	–	1.2	V
Low-Side On-Resistance	R_{ONL}	V_{BB} ≥ 7 V, I_{OUT} = 1 A, T_J = 25°C, MXI[4:0] = 3…31	–	500	600	mΩ
		V_{BB} = 13.5 V, I_{OUT} = 1 A, T_J = 150°C, MXI[4:0] = 3…31	–	900	1100	mΩ
		V_{BB} ≥ 7 V, I_{OUT} = 150 mA, T_J = 25°C, MXI[4:0] = 0…2	–	1200	1800	mΩ
		V_{BB} = 13.5 V, I_{OUT} = 150 mA, T_J = 150°C, MXI[4:0] = 0…2	–	2100	3000	mΩ
Low-Side Body Diode Forward Voltage	V_{FL}	I_F = –1 A [1]	–	–	1.4	V
		I_F = –0.1 A [1]	–	–	1.2	V
Output Leakage Current [1]	I_{LO}	GTS = 0, RESETn = 1, DIS = 1, V_O = V_{BB}	–	65	120	µA
		GTS = 0, RESETn = 1, DIS = 1, V_O = 0 V	–200	–120	–	µA
		GTS = 1 or V_{RESETn} < 0.5 V, V_O = V_{BB}	–	<1.0	20	µA
		GTS = 1 or V_{RESETn} < 0.5 V, V_O = 0 V	–20	<1.0	–	µA
Output Slew Rate	dV_O/dt	SLEW = 0, V_{BB} = 13.5 V	–	100	–	V/µs
		SLEW = 1, V_{BB} = 13.5 V	–	30	–	V/µs

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 28 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
CURRENT CONTROL						
System Clock Period	t_{OSC}		47.5	50	52.5	ns
Blank Time	t_{BLANK}	Default power-up value	3.32	3.5	3.68	µs
		Programmable range	1	–	3.5	µs
PWM Frequency	f_{PWM}	Default power-up value	18.32	19.20	20.24	kHz
		Programmable range	16.4	–	27.8	kHz
Bridge PWM Period	t_{PWM}	Default power-up value, DS = 0	49.4	52.0	54.6	µs
		Programmable range, DS = 0	36.0	–	60.8	µs
Maximum PWM On Time	t_{PMX}	Default power-up value	–	32	–	µs
		Programmable range	disable	–	56	µs
Bridge PWM Dither Step Period	Δt_{PWM}	Default power-up value	–0.19	–0.20	–0.21	µs
		Programmable range	–0.2	–	–1.6	µs
Bridge PWM Dither Dwell Time	t_{DIT}	Default power-up value	0.95	1.00	1.05	ms
		Programmable range	1	–	10	ms
Current Trip Point Error [2]	E_{ITrip}	MXI[4:0] = 3…31	–	–	±10	%
		MXI[4:0] = 0…2	–	–	±15	%
LOGIC INPUT AND OUTPUT – DC PARAMETERS						
Input Low Voltage	V_{IL}		–	–	0.3 × V_{LIO}	V
Input Low Voltage for Sleep Mode	V_{ILS}	RESETn input only	–	–	0.5	V
Input High Voltage	V_{IH}		0.7 × V_{LIO}	–	–	V
Input Hysteresis	V_{IHys}		100	300	–	mV
Input Pull-Up Resistor	R_{PU}	STRn	–	80	–	kΩ
Input Pull-Down Resistor	R_{PD}	SDI, STEP, DIR, RESETn	–	80	–	kΩ
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OL} = –1 mA [1]	V_{LIO} – 0.4	–	–	V
Output Leakage [1] (SDO)	I_{OSD}	0 V < V_O < V_{LIO}, STRn = 1	–1	–	1	µA
Output Leakage [1] (DIAG)	I_{ODI}	0 V < V_O < 9 V	–	–	1	µA
LOGIC INPUT AND OUTPUT – DYNAMIC PARAMETERS [3]						
Reset Pulse Width	t_{RST}		1.5	–	8	µs
Reset Shutdown Pulse Width	t_{RSD}		40	–	–	µs
Wake Up From Sleep	t_{EN}		–	–	1	ms
Interface Ready From Sleep	t_{IR}		–	–	1.1	ms
Input Pulse Filter Time	t_{PIN}	STEP, DIR pin	–	1	–	µs

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 28 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
SERIAL INTERFACE – DYNAMIC PARAMETERS [3]						
Clock High Time	t_{SCKH}	A [3]	50	–	–	ns
Clock Low Time	t_{SCKL}	B [3]	50	–	–	ns
Strobe Lead Time	t_{STLD}	C [3]	150	–	–	ns
Strobe Lag Time	t_{STLG}	D [3]	30	–	–	ns
Strobe High Time	t_{STRH}	E [3]	350	–	–	ns
Data Out Enable Time	t_{SDOE}	F [3]	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G [3]	–	–	30	ns
Data Out Valid Time from Clock Falling	t_{SDOV}	H [3]	–	–	45	ns
Data Out Hold Time from Clock Falling	t_{SDOH}	I [3]	5	–	–	ns
Data In Setup Time to Clock Rising	t_{SDIS}	J [3]	15	–	–	ns
Data In Hold Time from Clock Rising	t_{SDIH}	K [3]	10	–	–	ns
DIAGNOSTICS AND PROTECTION						
VBB Overvoltage Threshold [5]	V_{BBOV}	V_{BB} rising	32	34	36	V
VBB Overvoltage Hysteresis [5]	$V_{BBOVHys}$		2	–	4	V
VBB Undervoltage Threshold [5]	V_{BBUV}	V_{BB} falling	4.7	4.9	5.1	V
VBB Undervoltage Hysteresis	$V_{BBUVHys}$		100	200	300	mV
VBB POR	V_{BBPOR}	V_{BB} falling	–	3.2	3.7	V
VCP Undervoltage Threshold	V_{CPUVH}	V_{CP} falling	4.3	4.5	4.85	V
VCP Undervoltage Hysteresis	$V_{CPUVHHys}$		200	350	500	mV
High-Side Overcurrent Threshold	I_{OCH}		1.6	2.2	3	A
High-Side Overcurrent Limit	I_{LIMH}	Active during t_{OC}	2.4	5.5	8	A
High-Side Overcurrent Margin	I_{MAR}	$I_{MAR} = I_{LIMH} - I_{OCH}$	300	–	–	mA
Low-Side Overcurrent Threshold	I_{OCL}	MXI[4:0] = 3…31	1.6	2.2	3	A
		MXI[4:0] = 0…2	0.35	0.55	0.75	A
Overcurrent Fault Delay	t_{OC}	Default fault delay	1.9	2.0	2.1	µs
Open Load Current Threshold	E_{IOC}	OLT = 0 (Default)	8	14	25	mA
		OLT = 1	21	28	39	mA
DIAG Output: Clock Division Ratio	N_D			256000		
DIAG Output: Temperature Range	V_{TJD}	DG[1:0] = 1,0	–	1440	–	mV
DIAG Output: Temperature Slope	A_{TJD}	DG[1:0] = 1,0	–	–3.92	–	mV/°C
Hot Temperature Warning Threshold	T_{JWH}	Temperature increasing	125	135	145	°C
Hot Temperature Warning Hysteresis	T_{JWHHys}		–	15	–	°C
Overtemperature Shutdown	T_{JF}	Temperature increasing	170	–	180	°C
Overtemperature Hysteresis	T_{JHys}	Recovery = $T_{JF} - T_{JHys}$	–	15	–	°C

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.
[2] Current Trip Point Error is the difference between actual current trip point and the target current trip point, referred to maximum full scale (100%) current: $E_{ITrip} = 100 \times (I_{TripActual} - I_{TripTarget}) / I_{FullScale}$ %.
[3] Timing parameter letters refer to Interface Timing Diagrams.
[4] Function is correct but parameters are not guaranteed above or below the general limits (5.5 to 28 V).
[5] Outputs disabled if $V_{BB} > V_{BBOV}$ or $V_{BB} < V_{BBUV}$ or $V_{CP} < V_{CPUV}$.

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TIMING DIAGRAMS

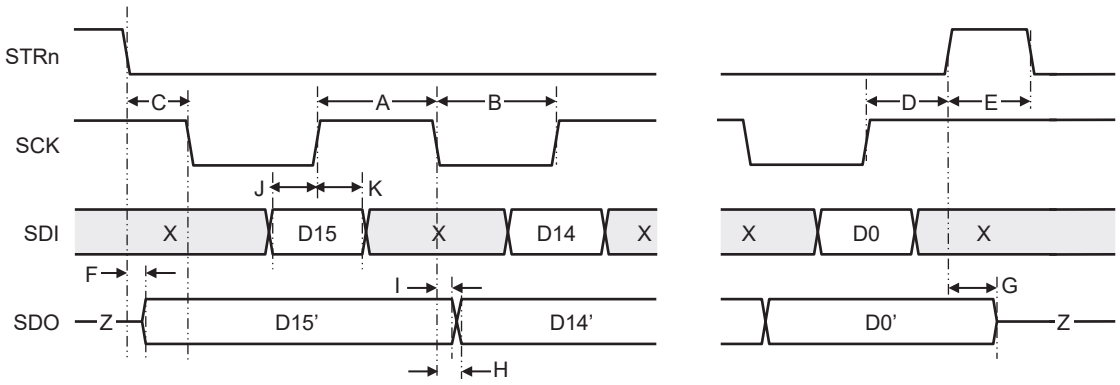

Figure 2: Serial Interface Timing

(X = don't care; Z = high impedance (tri-state)

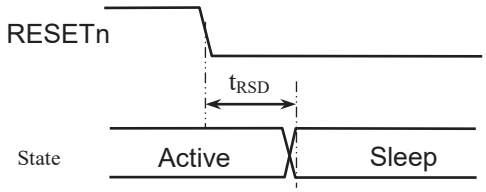

Figure 3a: Transition to Sleep (RESETn)

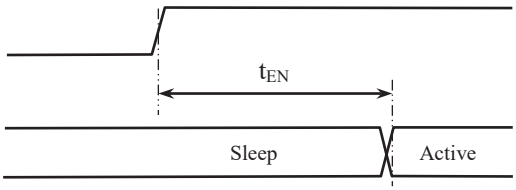

Figure 3b: Transition from Sleep (RESETn)

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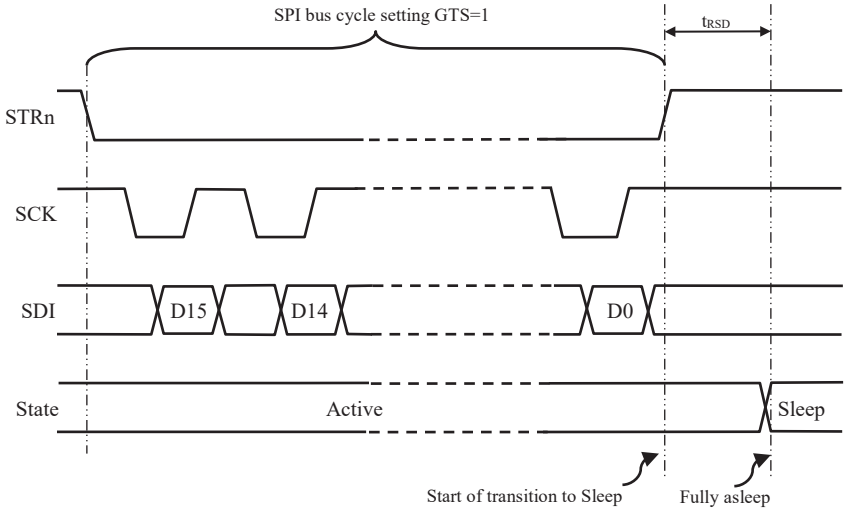

Figure 4a: Transition to Sleep (SPI)

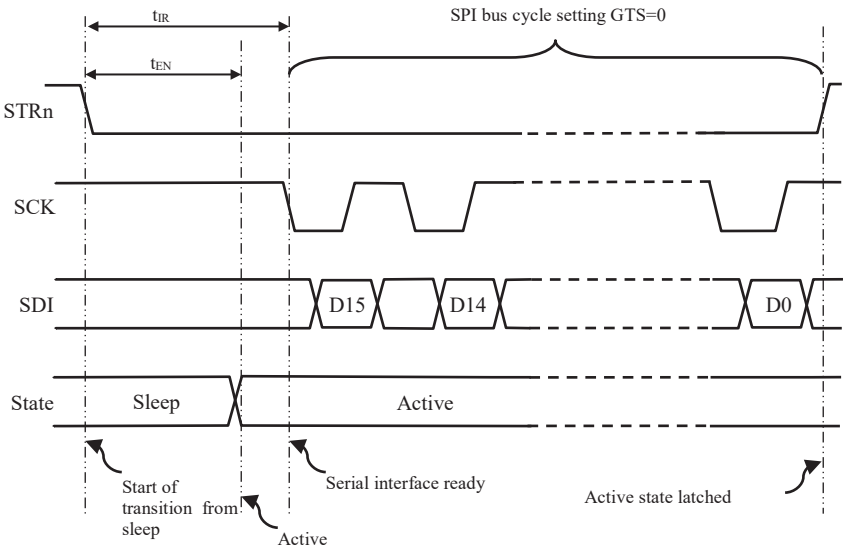

Figure 4b: Transition from Sleep (SPI, Active State Latched)

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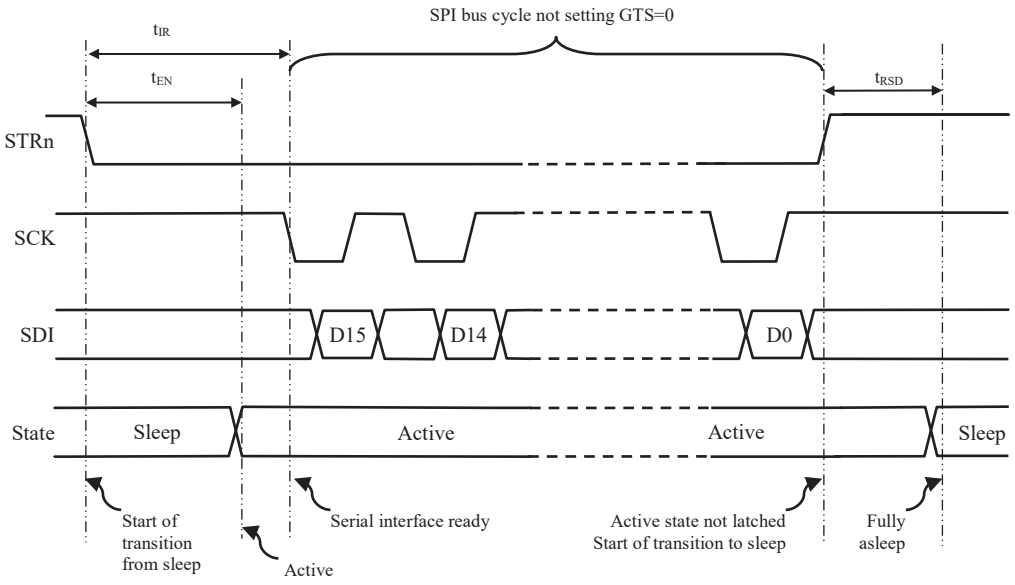

Figure 4c: Transition from Sleep (SPI, Active State Not Latched)

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FUNCTIONAL DESCRIPTION

The AMT49700 is an automotive stepper motor driver suitable for high temperature applications such as headlamp bending and leveling, throttle control, and gas recirculation control. It is also suitable for other low current stepper applications such as air conditioning and venting. It provides a flexible microstepping motor driver controlled through an SPI-compatible interface. The stepper motor can be controlled to provide single step movement, with adjustable microstep resolution for fine positioning control, or programmable multistep sequencing. The programmable step sequencer provides independent motor acceleration, deceleration, start speed, run speed, and number of steps with a single SPI command.

The SPI-compatible serial interface also allows the selection of step mode, configuration of motor control parameters, and programming of diagnostic thresholds.

A single diagnostic output provides simple indication of a fault condition and detailed diagnostic information can be read from the serial interface output.

The two DMOS full-bridges are capable of driving bipolar stepper motors in full-, half-, quarter-, eighth- and sixteenth-step modes, at up to 28 V, with phase current up to ±1.6 A but limited by power dissipation and ambient temperature. For most applications, typical phase current is up to ±750 mA. The current in each phase of the stepper motor is regulated by a fixed-frequency peak-detect PWM current control scheme operating in an adaptive mixed decay mode. This provides reduced audible motor noise and increased step accuracy for a wide range of motors and operating conditions.

The outputs are protected from short circuits and features for open load detection are included. Chip level protection includes hot thermal warning, overtemperature shutdown, and overvoltage and undervoltage lockout.

To assist with EMC compliance, the output slew rate is controlled at two programmable levels and the bridge PWM frequency includes optional programmable dither to spread the EM energy in the frequency spectrum.

Terminal Functions

VBB: Main motor supply and chip supply for internal regulators and charge pump. Both VBB pins should be connected together and each decoupled to ground with a low ESR electrolytic capacitor and a good ceramic capacitor.

CP1, CP2: Pump capacitor connection for charge pump. Connect a 100 nF (50 V) ceramic capacitor, between CP1 and CP2.

VCP: Above supply voltage for high-side drive. A 100 nF (16 V) ceramic capacitor should be connected between VCP and VBB to provide the pump storage reservoir.

GND: Power and reference ground. Connect to GNDPA and GNDPB pins—see layout recommendations.

GNDPA, GNDPB: Bridge power grounds. Connect to GND—see layout recommendations.

OAP, OAM: Motor connection for phase A. Positive motor phase current direction is defined as flowing from OAP to OAM.

OBP, OBM: Motor connection for phase B. Positive motor phase current direction is defined as flowing from OBP to OBM.

SDI: Serial data input. 16-bit serial word, input MSB first.

SDO: Serial data output. High impedance when the STRn input is high. Outputs the FF bit of the Status register, the fault flag, as soon as the STRn input goes low.

SCK: Serial clock. Data is latched in from SDI on the rising edge of SCK. There must be 16 rising edges per write and SCK must be held high when the STRn input changes.

STRn: Serial data strobe and serial access enable. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

DIAG: Diagnostic output. Function selected through serial interface. Default is fault output.

RESETn: Resets faults when pulsed low for a duration compliant with the Reset Pulse Width (t_{RST}). Forces low-power shutdown (sleep) when held low for more than the Reset Shutdown Width (t_{RSD}). Can be pulled to VBB with a 33 kΩ resistor.

STEP: STEP logic input. Motor advances on rising edge. Filtered input with hysteresis.

DIR: Direction logic input. Direction changes on next STEP rising edge. When high, the Phase Angle Number is increased on the rinsing edge of STEP. Has no effect when using the serial interface. Filtered input with Hysteresis.

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Stepper Motor Motion Control

The AMT49700 provides two methods of motion control, a single-step mode and a programmed step-sequence mode. Single-step mode can be controlled either by STEP and DIR terminals or through the serial interface. Step-sequence mode can only be controlled through the serial interface.

SINGLE-STEP CONTROL

The single-step mode is accessed by writing a step change value into the SC[5:0] variable. The step change value is a two's complement (2'sC) number, where a positive value moves the motor forward by a number of 1/16th microsteps and a negative value moves the motor backwards by a number of 1/16th microsteps. For example, for a full-step forwards the decimal number 16 would be written to SC. For a half step backwards the number -8 would be written to SC. Further details and examples are provided in the applications section.

The Step and Direction control mode uses the STEP and DIR terminals. When using Step and Direction mode to control stepper motor, the AMT49700 automatically increases or decreases the Step Angle Number according to the step sequence associated with the selected step mode. The default step mode, reset at power-up or after a power-on reset, is half step. Full-, quarter-, and sixteenth-step sequences are also available when using the STEP and DIR inputs and are selected by the contents of MS[2:0].

STEP-SEQUENCE CONTROL

The step-sequence mode provides the ability to command the motor to run a number of steps in either direction following a programmable accelerate, run and decelerate profile. The acceleration, deceleration, running step rate, starting step rate, total number of steps and direction can all be configured independently through the serial interface by writing to the following variables:

ACC[5:0]:	Acceleration in Full steps/s^2
DEC[5:0]:	Deceleration in Full steps/s^2
SSR[5:0]	Starting Step rate in Full steps/s
RSR[5:0]	Running Step rate in Full steps/s
DIR	Direction
NSM[7:0]	Most significant 8 bits of the step count
NSL[7:0]	Least significant 8 bits of the step count

All step profile parameters are based on full step units except the target steps, NSM[7:0] and NSL[7:0]. The actual motor speed, acceleration, deceleration and number of steps will always be the same regardless of the selected microstep resolution.

The sequence will start or change when STRn goes high at the end of the transfer of NSL[7:0], the least significant 8 bits of the step count number. When a programmed step seqence is complete, the motor will remain stopped until the end of the next NSL[7:0] transfer. When a programmed step seqence is in progress, the STEP and DIR inputs are ignored. The logic level on the DIR input has no effect on step-sequence control. In this operating mode, the direction is only defined by the DIR bit. Operational direction can be read on DIRR in Register 13 via serial interface either in the STEP and DIR mode or the Motion Control mode. The DIRR data is latched at the STRn signal taking low.

Figure 5 shows the definition of the basic step profile parameters and the sequence that occurs when the least significant 8 bits of the step count number are written. From a stationary state, the AMT49700 will begin by stepping the motor at the programmed start rate for the first step. The following steps will increase in step rate according to the programmed acceleration until the motor reaches the run step rate. At each step, the total step count remaining is reduced by one. The motor continues to be stepped at the run step rate until the step count reaches the number of steps required to decelerate the motor based on the run rate, the start rate and the deceleration factor. At this point the step rate is reduced at each step according to the programmed deceleration until the motor reaches the start step rate. Once the start step rate is achieved, the motor is stopped.

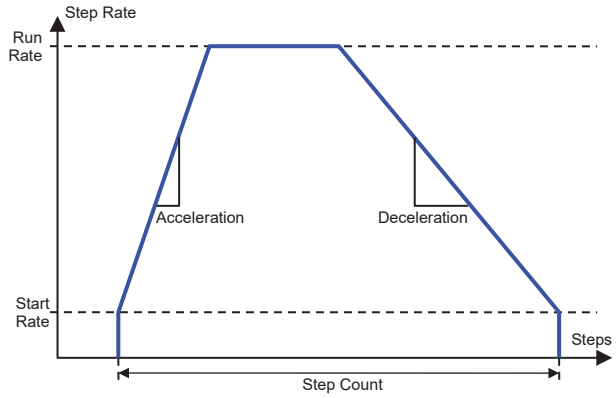

Figure 5: Step Profile Parameters

It is possible to change the variables when the step sequence is in progress, but the changes only take effect when the lsb of the step count is written. The effect of any change will depend on the present state of the step sequence. In each case, the AMT49700

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will either continue running at the run step rate, accelerate the motor or decelerate the motor. However, note that changing the deceleration rate to zero, when the motor is running with a motion profile, will cause the motor to run continuously.

Three additional single bit commands, END, STP, and BRK, are available to bring the motor to a halt without having to change the step sequence variables. When set to 1, the END bit will immediately decelerate the motor to stop, based on the programmed deceleration value and the start run rate, regardless of the present speed. change in speed, or remaining step count. When set to 1, the STP bit will immediately cease any step sequence and stop and hold the motor. The BRK bit provides the additional ability to stop driving current into the motor and will short the windings to provide some amount of dynamic braking. Further details and examples are provided in the applications section. If a motion profile is initiated while either END or STP bits are set, the command is accepted and the CR bit is set low. The profile will not be imitated until the STP or END bits are set low.

Driving a Stepper Motor

A two-phase stepper motor is made to rotate by sequencing the relative currents in each phase. In its simplest form, each phase is fully energized in turn by applying a voltage to the winding. For more precise control of the motor torque across temperature and voltage ranges, current control is required. For efficiency, this is usually accomplished using PWM techniques. In addition, current control also allows the relative current in each phase to be controlled, providing more precise control over the motor movement and hence improvements in torque ripple and mechanical noise.

For bipolar stepper motors, the current direction is significant, so the voltage applied to each phase must be reversible. This requires the use of a full-bridge (also known as an H-bridge), which can switch each phase connection to supply or ground.

Phase Current Control

In the AMT49700, current to each phase of the two-phase bipolar stepper motor is controlled through a low-impedance n-channel DMOS full-bridge. This allows efficient and precise control of the phase current using fixed-frequency pulse-width-modulation (PWM) switching. The full-bridge configuration provides full control over the current direction during the PWM on-time and the current decay mode during the PWM off-time. The AMT49700 automatically controls the bridge decay mode to provide the optimum current control completely transparent to the user.

Each leg (high-side, low-side pair) of each bridge is protected from shoot-through by a fixed dead-time. This is the time between switching off one MOSFET and switching on the complementary MOSFET. Cross-conduction is prevented by lockout logic in each driver pair.

Except for the half-step uncompensated mode, the phase currents and, in particular, the relative phase currents are defined by the phase current table (Table 3). This table defines the two phase currents at each microstep position. For each of the two phases, the currents are measured in the bridge transistors on the AMT49700. The target current level is defined by the output from the digital-to-analog converter (DAC) for that phase.

The actual current delivered to each phase at each step angle is determined by the value of the MXI[4:0] variable and the contents of the phase table. For each phase, the value in the phase table is passed to the DAC, which uses MXI[4:0] as the reference 100% level (code 63) and reduces the current target depending on the DAC code. The output from the DAC is used as the input to the current comparators. The controlled step angle can be read out via serial interface, SA[5:0]. The SA value is equivalent to the Step number in sixteenth step (Table 3).

The one exception is the uncompensated half-step mode. In this mode, the current in each phase at the half-step positions (8, 24, 40, and 56), with both phases active, will be the same level as at the full-step detent positions (0, 16, 32, and 48), with one phase active.

Low-side on-resistance (R_{ONL}) is automatically modified at maximum phase current settings of 120 mA or less (MXI[4:0] = 0…2) to maintain current-sense accuracy. High-side on-resistance (R_{ONH}) remains constant across all maximum phase current settings.

The current comparison is ignored at the start of the PWM on-time for a duration referred to as the blank time. The blank time is necessary to prevent any capacitive switching currents from causing a peak current detection.

The PWM on-time starts at the beginning of each PWM period. The current rises in the phase winding until it reaches the required peak current level. At this point, the PWM off-time starts and the bridge is switched into fast decay. The current continues to be monitored. When the current drops below the peak current level, the bridge is switched into slow decay for the remainder of the PWM period. This mixed decay technique automatically adapts the current control to a wide range of motors and operating conditions in order to minimize motor torque ripple and motor noise. It also provides the lowest motor dissipation and highest motor efficiency over a wide range of voltage and temperature conditions.

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The AMT49700 includes a programmable maximum PWM-on time limiter. In some cases, for example a phase short to ground, the motor current does not flow through the low side peak current sensor. In this case, the current measured by the peak current detector will not to reach the peak current threshold and the bridge would remain in the PWM-on state. This may allow the current to increase until it is limited only by the supply voltage and motor resistance. The maximum on time is set using the PM[4:0] variable as a maximum number of PWM periods from 1 to 56 in steps of 8 cycles. Setting PM[4:0] to 0 will disable the maximum PWM-on time limit. If the PWM-on time reaches the programmed limit the bridge will be disabled as if an overcurrent had been detected and an overcurrent will be indicated in the Diagnostic register for the high-side output of the opposite phase to the previously active phase. For example, if OAP is driven high and OAM driven low when the PWM-on time limit is reached then the AMH bit would be set indicating a possible short between OAM and GND and the bridge control follows the sequence as for an overcurrent detection.

Phase Current Table

Except for the uncompensated half step mode, the relative phase currents are defined by the phase current table, Table 3. This table contains 64 lines and is addressed by the step angle number, where step angle 0 corresponds to 0° or 360°. The step angle number is generated internally by the step sequencer, which is controlled by the motion controller or by the step change value from the serial input. The step angle number determines the motor position within the 360° electrical cycle and a sequence of step angles determines the motor movement. Note that there are four full mechanical steps per 360° electrical cycle.

Each line of the phase current table has a 6-bit value, per phase, to set the DAC level for each phase plus an additional bit, per phase, to determine the current direction in each phase. The step angle number sets the electrical angle of the stepper motor in sixteenth microsteps, approximately equivalent to electrical steps of 5.625°.

On first power up, after a power-on reset or after sleep, the step angle number is set to 8, equivalent to the electrical 45° position, except for full-step single phase drive where the step angle number is set to 0. This position is defined as the “home” position.

When using the programmable step sequencer to control the stepper motor, the AMT49700 automatically increments or decrements the step angle according to the step angle sequence associated with the selected microstep mode. The default microstep mode is compensated half step. Full single-phase-, full two-phase-, uncompensated half-, quarter-, eighth- and sixteenth step sequences are also available when using the programmable step sequencer and are selected by the contents of the MS[2:0] variable.

When using single-step control option to control the stepper motor, a 6-bit step change value is written to SC[5:0] to increment or decrement the step angle. The step change value is a two’s complement (2’sC) number, where a positive value increments the step angle and a negative value decrements the step angle. A single step change in the step angle is equivalent to a single 1/16th microstep. Therefore, for correct motor movement, the step change value should be restricted to no greater than 16 steps positive or negative.

This facility enables full control of the stepper motor at any microstep resolution up to 16th step, plus the ability to change microstep resolution “on-the-fly” from one microstep to the next. The only restriction is that the single-step control mode cannot operate in uncompensated half-step mode. The microstep mode selection set by MS[2:0] has no effect in single-step control.

In both control cases, the resulting step angle number is used to determine the phase current value and current direction for each phase based on the phase current table.

PWM Frequency

The base frequency of the bridge PWM signal is fixed by the value of the base PWM period, t_{PW}. This base frequency can be altered by the frequency dither function described below.

The period of the PWM frequency is set by the PW[4:0] variable. The six bits of PW contain a positive integer that determines the PWM period derived by division from the system clock.

The PWM period is defined as:

$$t_{PW} = 36\ \mu s + (n \times 0.8)\ \mu s$$

where n is a positive integer defined by PW[4:0]

For example, when PW[4:0] = [1 0100], then $t_{PW} = 52\ \mu s$ and the PWM frequency is 19.2 kHz.

The range for the base PWM frequency is 16.4 kHz to 27.8 kHz. The accuracy of the PWM frequency is defined by the system clock accuracy.

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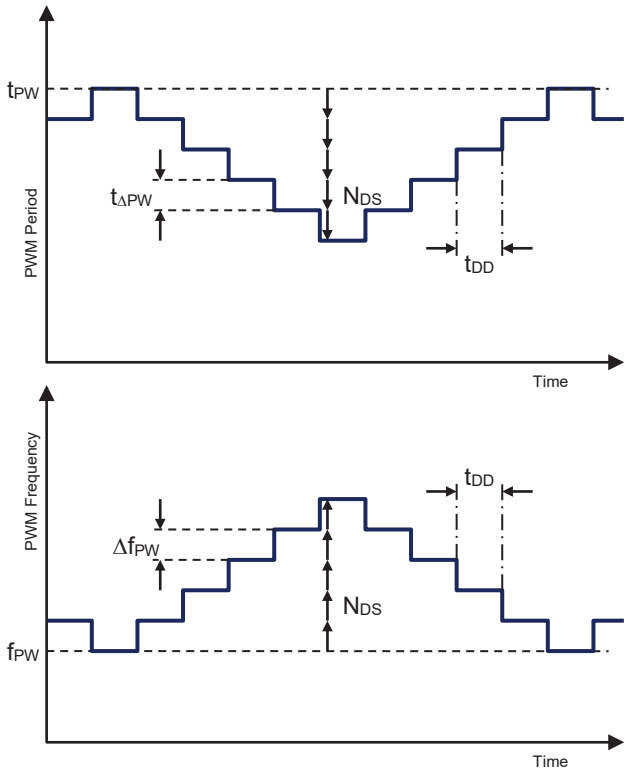

Figure 6: PWM Frequency Dither

PWM Frequency Dither

The AMT49700 includes an optional PWM frequency dither scheme that can be used to reduce the peak radiated and conducted electromagnetic (EM) emissions. This is accomplished by stepping the PWM period in a triangular pattern in order to spread the EM energy created by the PWM switching. There are three programmable variables that can be used to adjust the frequency spreading for different applications. These are the dither step period, $t_{\Delta PW}$, dwell time, t_{DD}, and the number of steps in the pattern, N_{DS}. These are identified in Figure 6.

Figure 6 shows the dithered period on top and the corresponding frequency below. The PWM frequency at any time is defined by the PWM period. The base PWM period, t_{PW}, is indicated as is the resulting base frequency, f_{PW}.

The dither step period, $t_{\Delta PW}$, is the incremental change in PWM period at each dither step and is defined by:

$$t_{\Delta PW} = -0.2 - (n \times 0.2)\ \mu s$$

where n is a positive integer defined by DP[2:0].

Following each change, the PWM period will remain at the new value for the duration of the dither dwell time, selected as 1 ms, 2 ms, 5 ms, or 10 ms by the contents of the DD[1:0] variable.

The number of dither steps, N_{DS}, is the value in the DS[3:0] variable. Starting at the base PWM period, the PWM period will decrease by the dither step period N_{DS} times then increase by the same amount and number of steps before restarting the cycle. N_{DS} can have a value between 0 and 15. A value of 0 will disable PWM frequency dither. The minimum PWM period in any case is 18 µs. If the frequency dither settings attempt to reduce the PWM period below 18 µs, then it will be held at 18 µs until the dther sequence brings the required value above 18 µs again.

As the frequency shift is defined by a fixed period change, the change in frequency will be slightly different for each step, but the frequency spreading effect will still be effective.

Low-Power Sleep Mode

The AMT49700 can be put into a low power sleep mode by holding the RESETn input low for a duration of at least the Reset Shutdown Pulse Width, t_{RSD} (Figure 3a) or setting the GTS bit to 1 via the serial interface (Figure 4a). If GTS is used, the transition to sleep starts on the rising edge of STRn at the end of the serial write cycle and is completed one Reset Shutdown Pulse Width later. In combination, the two means of initiating sleep behave as detailed in Table 1.

Table 1: Sleep Mode Logic

RESETn	GTS Bit	Mode
0	0	Sleep
0	1	Sleep
1	0	Normal
1	1	Sleep

In sleep mode, the outputs are disabled and the internal regulators are switched off to minimize current drain from the battery supply. If the initiation of sleep mode is successful, the DIAG output is set high; if unsuccessful, it is set low. This behavior occurs regardless of the value of the DGS[1:0] variable and may be used to confirm that a command to enter or exit sleep mode has been successful. The DIAG output state is not defined and should not be read during the Reset Shutdown Pulse Width, t_{RSD}, or Wake from sleep, t_{EN}, periods.

If sleep mode is initiated by taking RESETn low, it will be exited on the following rising edge on RESETn per Figure 3b. If sleep mode is initiated by setting GTS to 1, the part will start to wake up on the first falling edge on STRn as detailed in Figure 4b. The

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serial transfer associated with the STRn falling transition initiating wake up must set GTS to 0, otherwise active mode will not be latched and the device will revert to sleep at the end of the cycle per Figure 4c.

Unlike other bus cycles, the first transfer after coming out of sleep mode must satisfy the constraint that the first falling edge on SCK does not occur until at least an Interface Ready period, t_{IR}, after the falling edge on STRn. This allows the internal regulators to power up and the interface logic to become active. During t_{IR}, any switching commands on STEP, DIR, STRn, SCK, and SDI should be avoided to avoid unpredictable operation.

If sleep mode is initiated by setting GTS to 1 and then RESETn is taken low, exit from sleep requires that RESETn is taken high prior to setting GTS to 0.

Diagnostics

The AMT49700 integrates a number of diagnostic features to protect the driver and load as far as possible from fault conditions and extreme operating environments. When a fault condition is detected or confirmed then a fault state exists and the fault is captured by the diagnostic register and the status register. There are two types of fault conditions, defined as dynamic and static.

Dynamic fault conditions are those that only exist for a short duration, either due to some action being taken by the AMT49700 that removes the fault condition, or the fault is only detectable at specific instants. Fault states generated in response to Dynamic faults are latched to ensure that such faults are reported through the diagnostic output terminal, DIAG, and to ensure that dangerous conditions cannot return or persist to damage the AMT49700 or the load.

Table 2: Fault State Table

Diagnostic	Action	Latched
VBB Overvoltage	Disable outputs	No
VBB Undervoltage	Disable outputs	No
VCP Undervoltage	Disable outputs	No
Temperature Warning	Flag fault only	No
Overtemperature	Disable outputs	No
Bridge Short	Disable output	Yes
Bridge Open	Flag fault only	Yes
Serial Interface Fault	Flag fault only	No

Bridge overcurrent (bridge short condition) and bridge open detect faults are categorized as Dynamic.

Static faults states are those that only exist when the fault condition is present. When such a fault condition is removed, the fault state is no longer present.

In both cases, the fault is always captured independently by the diagnostic or status registers. The contents of these registers are not reset when the fault state clears and provide a record of all faults that have occurred since the last reset of the register in question. Any fault bits set to 1 in the Diagnostic or Status registers are reset by a Status or Diagnostic register reset described below. If any static faults persist following a reset action the relevant fault states and register bits will reflect this immediately after completion of the reset.

A number of these features automatically disable the current drive to protect the outputs and the load. Others only provide an indication of the likely fault status. Fault states and associated actions are listed in Table 2.

A single open-drain diagnostic output (DIAG) can be programmed through the serial interface to provide four different fault signals.

At power-up or after a power-on-reset, the DIAG terminal outputs a general fault flag, which goes low when a fault state is present. It indicates that a static fault condition is present or a dynamic fault condition has been detected and latched.

In addition to the general fault flag, the DIAG output can be programmed via the serial interface to output any of seven other optional fault indicators:

- A supply voltage error signal, which is low when a VBB overvoltage, VBB undervoltage or VCP undervoltage fault state is present.
- An open load indicator.
- A voltage that represents the silicon temperature.
- A logic level version of the PWM switching on phase A.
- The internal step signal from the sequencer to the stepper driver.
- A step sequence activity indicator which is low when the SSA bit in the Status register is 1 and high when SSA is zero. This indicates when a programmed sequence of steps is actively running.
- A divided version of the internal system clock giving 78.125 Hz

The DIAG terminal will survive a maximum applied voltage of 40 V per the Absolute Maximum Ratings table, but switches into a high impedance state when the applied voltage exceeds approximately 16 V (regardless of programmed terminal function

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or device status). On-state drive capability and off-state leakage current limits are defined in the Electrical Characteristics table by the V_{OL} and I_{ODI} parameters respectively and may be used to calculate a suitable pull-up resistance. In the majority of applications, a resistor in the range 10 kΩ to 20 kΩ is suitable.

System Diagnostics

At the system level, the supply voltages and chip temperature are monitored.

SUPPLY VOLTAGE MONITORS

The main supply VBB, the charge pump voltage VCP, and the internal supply voltages (derived from VBB but not externally accessible) are monitored—the main supply for overvoltage and undervoltage, the others for undervoltage only.

- If the main supply voltage, V_{BB}, rises above its overvoltage threshold, V_{BBOV}, the AMT49700 disables the outputs, drives the general fault flag (DIAG) low and sets the OV bit in the Status register to 1. When the main supply voltage falls below its overvoltage threshold, V_{BBOV} - $V_{BBOVHys}$, the outputs are re-enabled, the general fault flag goes high, and the OV bit remains set in the status register until cleared.
- If the main supply voltage, V_{BB}, falls below the VBB undervoltage threshold, V_{BBUV}, the AMT49700 disables the outputs, drives the general fault flag (DIAG) low, and sets the UV bit in the Status register to 1. If V_{BB} remains above the VBB POR threshold, V_{BBPOR}, but is low enough such that the I/O voltage is less than the programmed value, it is possible that the external microcontroller may not be able to communicate with the AMT49700 through the serial interface. However, in this case, all register states (including step angle) are retained. When V_{BB} rises above the undervoltage threshold, V_{BBUV} + $V_{BBUVHys}$, and no other faults are present, the outputs are re-enabled, the general fault flag goes high and the UV bit remains set in the status register until cleared.
- If the output of the charge pump, V_{CP}, falls below its undervoltage threshold, V_{CPUV}, the AMT49700 disables the outputs, drives the general fault flag (DIAG) low, and sets the UV bit in the Status register to 1. When the charge pump output rises above its threshold, V_{CPUV} + $V_{CPUVHys}$, and no other faults are present, the outputs are re-enabled, the general fault flag goes high, and the UV bit remains set in the status register until cleared.
- If V_{BB} falls below the VBB power-on reset (POR) level and the internal logic supply voltages derived from V_{BB} drop below acceptable levels, the AMT49700 is completely disabled. DIAG is set low and held in this state for as long as the supply voltage permits. When the internal supply voltages rise to acceptable levels, a power-on reset takes place, the POR and FF bits are set to 1, and all other register bits are set to their default state. The VBB POR threshold, $V_{BBPO}R$, is an approximate value derived from the internal logic supply undervoltage threshold and the regulator dropout voltage. The AMT49700 is guaranteed not to be disabled if V_{BB} remains above the maximum value of V_{BBPOR}. The internal logic supply undervoltage threshold is set to guarantee that the internal logic will remain fully operational and correct down to the minimum value of the threshold.

If any of these supply fault states are present, and either the general fault flag or the supply fault flag is selected for output on DIAG, then DIAG will be low.

When applying power or when activating from sleep mode, the outputs should remain inactive for at least the wakeup from reset time, t_{EN}, to allow the internal charge pump and regulator to reach their full operating state.

The output drive MOSFETs of the AMT49700 remain protected from short circuits down to the VBB undervoltage level. However, when V_{BB} is less than 5.5 V, the overcurrent thresholds cannot be guaranteed to meet the precision specified at higher supply voltage. In addition, the open load detection may indicate a fault depending on the motor and load characteristics.

TEMPERATURE MONITORS

Two temperature thresholds are provided: a hot warning and an overtemperature shutdown.

- If the chip temperature rises above the hot temperature warning threshold (T_{JW}), the hot warning bit (TW) is set to 1 in the Status register. No action is taken by the AMT49700. When the temperature drops below T_{JW} by more than the hysteresis value (T_{JWHys}), the fault state is cleared, but the TW bit remains at1 in the Status register until reset.
- If the chip temperature rises above the overtemperature threshold (T_{JF}), the overtemperature bit (OT) is set to 1 in the Status register, and the AMT49700 disables the outputs to try to prevent a further increase in the chip temperature. When the temperature drops below T_{JF} by more than the hysteresis value (T_{JFHys}), the fault state is cleared, and the outputs re-enabled. The OT bit remains at 1 in the Status register until reset.

If either of these supply fault states is present and the general fault flag is selected for output on DIAG, then DIAG will be low.

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Bridge and Output Diagnostics

The AMT49700 includes monitors that can detect a short to supply or a short to ground at the motor phase connections. These conditions are detected by monitoring the current from the motor phase connections through the bridge to the motor supply and to ground. In addition, a PWM-on time limiter is provided to ensure that any motor phase short to ground events do not cause the current to increase out of control indefinitely.

Low current comparators and timers are provided to help detect possible open load conditions.

SHORTED LOAD

If the supply voltage is high enough to drive the bridge current above the overcurrent thresholds, a short across the load may be indicated by concurrent overcurrent fault states on both high-side and low-side MOSFETs.

OVERCURRENT FAULT BLANKING

All overcurrent conditions are ignored for the duration of the overcurrent detection delay time (t_{OC}) set between 1 and 4 µs by the contents of the TOC[1:0] variable. The overcurrent detection delay timer is started when an overcurrent condition is first detected. If the overcurrent condition is still present at the end of the overcurrent detection delay time, then an overcurrent fault state will be detected and latched. If the overcurrent condition is removed before the overcurrent detection delay time is complete, then the timer is reset and no fault is detected.

This prevents false overcurrent detection caused by supply and load transients. It also prevents false overcurrent detection from the current transients generated by the motor or wiring capacitance when a MOSFET is first switched on.

OVERCURRENT FAULT RESET AND RETRY

Once an overcurrent fault state has been detected, all outputs for the phase where the fault state is present are disabled until the fault state is reset by a register reset. In addition, if the Overcurrent Fault Action bit, OFA, is set to 0, any overcurrent fault states are reset every time a step occurs either on a single step or on each step of a step sequence. When the fault state is reset the outputs are re-enabled and if the general fault flag is selected for output on DIAG and there are no other faults, then DIAG will be allowed to go high. The same sequence is also applied if the PWM-on time reaches the maximum limit.

Resetting overcurrent fault states every time a step occurs allows automatic restart when the cause of the overcurrent is removed. If the cause of the overcurrent persists, the part will repeatedly cycle between overcurrent and attempted restart. In this condition, the device will not suffer damage, but if step demands are being applied at a high rate, the part may eventually shut down due to overtemperature.

If the OFA bit is set to 1, a step occurance does not reset overcurrent fault states and the automatic restart capability is disabled.

OPEN-LOAD DETECTION

Open load detection is carried out on both phases and if either phase current drops below the open load current threshold, I_{OL}, an open-load state is flagged. (I_{OL} is set to either 13 mA or 26 mA, according to the state of the OLT bit.)

Unfortunately, simple current monitoring is only viable for stationary motors where the current rises quickly. When motors are running at high speed, phase current rise time is severely affected by motor back emf and the current may not reach its peak until late in the step period. Consequently, if open-load current comparisons were to run continuously, false open-load states would be flagged for at least part of the step period in many instances. To avoid such false states, the open-load comparator outputs are only checked after the expiry of the open-load detect time. This lockout period starts each time a step occurs and has a duration of 10 ms to 40 ms selected by the contents of the TOL[1:0] variable. Additionally, the comparator output for each phase is only checked if the target current for that phase is greater than twice the open load threshold current.

The AMT49700 continues to drive the bridge outputs under an open-load condition. Any open-load fault state is cleared when any of four events occurs:

- A single step command is received by writing to the single step command register with DSR = 0 or a rising signal at the STEP terminal.
- A step sequence is started by writing to the step count lsb register with DSR = 0.
- The phase current reaches the PWM threshold level.
- The open-load detect time expires and the phase current is detected to have risen above the open-load current threshold.

When an open-load fault is present and a rising edge is detected on the STEP input, this will both clear the fault and step the motor by the programmed microstep value. This will avoid any systematic step count misalignment if the open-load state is only temporary and the controller continues to step the motor without taking any action on the open-load detection.

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False State Reset

Various mechanisms may be used to reset or partially reset the AMT49700.

RESET PULSE

Pulsing the RESETn input low for the duration of the reset pulse-width time, t_{RST}, clears all dynamic fault states, the General Fault Flag (DIAG) and the Diagnostic and Status registers provided no static faults remain present.

RESET COMMAND

Writing a 1 into the RST bit through the serial interface has the same effect as a pulse on the RESETn input. All dynamic fault states, the General Fault Flag (DIAG) and the Diagnostic and Status registers are cleared provided no static faults remain present.

SLEEP

Entering and then exiting sleep mode (via RESETn) clears all fault states (with the exception of POR and FF) and the General Fault Flag (DIAG). If GTS bit is written with DSR = 1, the recorded faults will not be cleared. Additionally, the Diagnostic and Status registers (with the exception of POR and FF) are cleared.

DIAGNOSTIC REGISTER READ

Reading the Diagnostic register via the serial interface, with DSR = 0, clears all overcurrent fault states and the overcurrent indicator bits in the Diagnostic register. Clearing all the overcurrent indicator bits will also clear the OCA and OCB bits in the Status register. Other bits in the Status register are not affected. Reading the Diagnostic register will have no effect on the state of the SSA bit. This is exclusively set or reset by the step sequence controller.

STATUS REGISTER READ

Reading the Status register with DSR = 0 via the serial interface clears all latched fault states other than those generated by overcurrent faults. If no other faults are present this action also clears the General Fault Flag and the fault bits in the register except for the overcurrent bits, OCB and OCA, which are derived from the contents of the overcurrent indicator bits in the Diagnostic register. If any static faults are present, e.g. overtemperature, then the corresponding fault bit will not be affected by reading the Status register and will remain set.

STEPPING

If the Overcurrent Fault Action bit, OFA, is set to 0 all overcurrent fault states and any associated fault indication on the General Fault Flag are cleared on every time a step occurs either on a single step. This provides a means of automatically attempting a restart. No bits in the Diagnostic or Status registers are cleared thereby allowing suspected faults to be investigated via the serial interface.

If the OFA is set to 1, any overcurrent fault state will remain and automatic attempts continue stepping are disabled. Any step sequence in progress will stop immediately.

DISABLE SERIAL RESET

The AMT49700 has a function to disable the fault reset action via the serial communication interface. When the DSR bit set to 1, AMT49700 will not clear the faults in Status and Diagnostics register by the reading command of Status and Diagnostics register. The CR and SSR are exclusively operated regardless of DSR. The reset command by RST bit or RESETn input pulse will operate as it is, even if DSR is set to 0.

Step Angle Reset

The step angle number may be set to its home value by writing a logic 1 to the SAR bit in the Control register. If using the SAR bit, the step angle number reset only takes place on the rising edge on STRn at the end of the write cycle. Repeatedly overwriting the value 1 to the SAR bit repeatedly resets the step angle. The SAR bit may be cleared by writing 0 via the serial interface. The SAR bit is also reset to 0 by a power-on reset. Maintaining SAR at 1 does not lock the step angle in the home condition, and any step or sequence commands received via the serial interface are obeyed. The step angle reset action will not be taken if the following conditions are present: DIS, OT, OV, UV, BRK, and any short fault.

Braking

The AMT49700 can be used to perform dynamic braking by setting the BRK bit to 1. If BRK is set to 1 and HLR = 0, all high-side MOSFETs are turned on and all low-side MOSFETs are turned off, effectively short-circuiting any back emf generated by the motor and creating a braking torque. If BRK is set to 1 and HLR = 1, all low-side MOSFETs are turned on and all high-side MOSFETs are turned off, producing a similar effect at the motor. During braking, motor current, I_{BREAK}, can be approximated by:

$$I_{BRAKE} = V_{BEMF} / R_L$$

where V_{BEMF} is the voltage generated by the motor and R_L is the resistance of the phase winding. Care must be taken during braking to ensure that the power MOSFET maximum ratings are not exceeded. When dynamic braking is commanded, open-load conditions cannot be detected because of the bridge configuration that is enforced (both ends of each motor winding held in the same state).

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SERIAL INTERFACE

Serial Registers Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: PWM Config	0	0	0	0	WR	PM4	PM3	PM2	PM1	PM0	PW4	PW3	PW2	PW1	PW0	P
						0	0	1	0	0	1	0	1	0	0	
1: PWM Config	0	0	0	1	WR		DP2	DP1	DP0	DD1	DD0	DS3	DS2	DS1	DS0	P
						0	0	0	0	0	0	0	0	0	0	
2: Current Config	0	0	1	0	WR	DIS	HLR	SLW	TBK1	TBK0	MXI4	MXI3	MXI2	MXI1	MXI0	P
						1	0	0	1	1	1	0	0	0	0	
3: Diagnostics Config	0	0	1	1	WR	DGS2	DGS1	DGS0		OLT	TOL1	TOL0	OFA	TOC1	TOC0	P
						0	0	0	0	0	1	0	0	0	1	
5: Single Step Control	0	1	0	1	WR	SAR				SC5	SC4	SC3	SC2	SC1	SC0	P
						0	0	0	0	0	0	0	0	0	0	
6: System Control	0	1	1	0	WR	GTS	RST	VLR	MS2	MS1	MS0	DSR	BRK	END	STP	P
						0	0	0	0	1	0	0	0	0	0	
7: Step Count (lsb)	0	1	1	1	WR	DIR	CRM	NSL7	NSL6	NSL5	NSL4	NSL3	NSL2	NSL1	NSL0	P
						0	0	0	0	0	0	0	0	0	0	
8: Step Count (msb)	1	0	0	0	WR			NSM7	NSM6	NSM5	NSM4	NSM3	NSM2	NSM1	NSM0	P
						0	0	0	0	0	0	0	0	0	0	
9: Acceleration	1	0	0	1	WR					ACC5	ACC4	ACC3	ACC2	ACC1	ACC0	P
						0	0	0	0	0	0	0	0	0	0	
10: Deceleration	1	0	1	0	WR					DEC5	DEC4	DEC3	DEC2	DEC1	DEC0	P
						0	0	0	0	0	0	0	0	0	0	
11: Min Step Rate	1	0	1	1	WR					SSR5	SSR4	SSR3	SSR2	SSR1	SSR0	P
						0	0	0	0	0	0	0	0	0	0	
12: Max Step Rate	1	1	0	0	WR					RSR5	RSR4	RSR3	RSR2	RSR1	RSR0	P
						0	0	0	0	0	0	0	0	0	0	
13: STEP Readback	1	1	0	1	R	DIRR				SA5	SA4	SA3	SA2	SA1	SA0	P
						0	0	0	0	0	0	0	0	0	0	
14: Mask	1	1	1	0	WR	OT	TW	OV	UV			OLB	OLA	OCB	OCA	P
						0	0	0	0	0	0	0	0	0	0	
15: Diagnostic	1	1	1	1	WR			BML	BMH	BPL	BPH	AML	AMH	APL	APH	P
						0	0	0	0	0	0	0	0	0	0	

	FF	POR	SE	CR	SSA	OT	TW	OV	UV			OLB	OLA	OCB	OCA	
Status	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	P

*Power-on reset value shown below each input register bit.

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A three-wire synchronous serial interface, compatible with SPI, can be used to control all features of the AMT49700. A fourth wire can be used, during a serial transfer, to provide diagnostic feedback and read back of the register contents.

The serial interface timing requirements are specified in the Electrical Characteristics table and illustrated in the Serial Interface Timing diagram, Figure 2. Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. A serial transfer is initiated by pulling the STRn terminal low.

STRn is normally high and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple slave units to use common SDI and SCK connections. Each slave then requires an independent STRn connection. The SDO output assumes a high-impedance state when STRn is high, allowing a common data readback connection. When driving devices running from a 5 V logic supply with VLR set to 0 (3.3 V I/O), it may be necessary to add a 2 kΩ pull-up resistor from SDO to that supply to ensure an adequate logic-high output voltage level is achieved.

When 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data.

If there are more than 16 rising edges on SCK or if STRn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without writing data to the registers. In addition, the Diagnostic and Status registers will not be reset and the SE bit will be set to indicate a data transfer error. This fault condition can be cleared by a subsequent valid serial write, a reset pulse on RESETn, a transition to sleep mode and back (RESETn or GTS), or a power-on-reset. If SE is cleared by RESETn pulse, another valid serial transfer is required to activate serial communication monitor.

The first four bits, D[15:12], in a serial word are the register address bits, giving the possibility of 16 register addresses. The fifth bit, WR (D[11]), is the write/read bit. Except for the read-only registers, when WR is 1, the following 10 bits, D[10:1], clocked in from the SDI terminal are written to the addressed register. When WR is 0, no data is written to the serial registers and the contents of the addressed register are clocked out on the SDO terminal.

The last bit in any serial transfer, D[0], is a parity bit that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transfer should always be an odd number. This ensures that there is always at least one bit set to 1 and one bit set to 0 and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

If the AMT49700 detects a parity error during a serial transfer, the data in question will not be written to the selected device register.

Register data is output on the SDO terminal msb first while STRn is low, and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF bit from the status register, is output as soon as STRn goes low.

Registers 15 (Diagnostic) contains detailed diagnostic indicators and is read only. If WR is set to 0, the content of the addressed register is clocked out on SDO D[10:1]. If WR is set to 1, no data are written to the addressed register and the content of the Status register is clocked out on SDO D[10:1].

In addition to the addressable registers, a read-only status register is output on SDO for all register addresses when WR is set to 1. For all serial transfers, the first five bits output on SDO will always be the first five bits from the status register.

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Serial Register Content

The serial data word is 16 bits, input msb first; the four bits are defined as the register address. This provides 16 addressable registers, 14 of which are read/write and 1 is read only. The registers are grouped as follows:

- PWM frequency and dither configuration
- Current and bridge configuration
- Diagnostic settings
- System function configuration
- Motor function control
- Fault mask
- Status and diagnostics

Register 0: PWM configuration

- PM[4:0], a 5-bit integer to set the max PWM on time
- PW[5:0], a 6-bit integer to set the PWM period

Register 1: PWM configuration

- DP[2:0], 3 bits to select the dither step period
- DD[1:0], 2 bits to select the dither dwell time
- DS[3:0], 3-bit integer to select the dither steps

Register 2: Current configuration

- DIS, Disables the motor drive outputs
- HLR, Selects the slow decay recirculation path
- SLW, Selects the bridge slew rate
- TBK[1:0], 2 bits
- MXI[4:0], 5 bits

Register 3: Diagnostics configuration

- DGS[1:0], 2 bits to select the output on DIAG
- OLT, Selects the open-load threshold current
- TOL[1:0], 2 bits to select the open-load detect timeout
- OFA, Selects action taken on an overcurrent fault
- TOC[1:0], 2 bits select the overcurrent fault delay time

Register 4: Unused

Register 5: Single Step Control

- SAR, Resets the step angle number to the home position
- SC[5:0], 5 bits to move the motor by a number of microsteps forwards or backwards

Register 6: System Control Settings

- GTS, initiates go-to-sleep function
- RST, Resets all faults and fault bits
- VLR, Selects the logic I/O voltage
- MS[2:0], 3 bits to select the microstep resolution
- DSR, Disable Serial Reset
- BRK, Applies brake by shorting windings
- END, Decelerates and ends any motor movement
- STP, Stops any motor movement

Register 7: Step count (lsb)

- DIR, Select the step direction
- CRM, Continuous Run Mode
- NSL[7:0], least significant 8 bits of step count

Register 8: Step count (msb)

- NSM[7:0], most significant 8 bits of step count

Register 9: Acceleration

- ACC[5:0], 6 bits to set the acceleration rate

Register 10: Deceleration

- DEC[5:0], 6 bits to set the deceleration rate

Register 11: Start Step Rate

- SSR[5:0], 6 bits to set the minimum step rate

Register 12: Running Step Rate

- RSR[5:0], 6 bits to set the running step rate

Register 13: STEP Readback

- DIRR, STEP Direction readback
- SA[5:0], 6 bits step angle readback

Register 14: Fault Mask

- The Fault Mask Register contains a fault mask bit for each fault bit in the status register other than FF, POR, and SE. If a bit is set to one in the mask register, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated and no fault flags or diagnostic bits will be set.

Register 15: Diagnostic (read only):

- Individual bits indicating overcurrent faults detected in each bridge MOSFET.

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Status and Diagnostic Registers

There is one read-only status register in addition to the 16 addressable registers. When any register transfer takes place, the first five bits output on SDO are always the most significant five bits of the status register regardless of whether the addressed register is being read or written (see serial timing diagram). The content of the remaining eleven bits will depend on the state of the WR bit input on SDI. When WR is 1, the addressed register will be written and the remaining eleven bits output on SDO will be the least significant ten bits of the status register and a parity bit. When WR is 0, the addressed register will be read and the remaining eleven bits will be the contents of the addressed register and a parity bit.

The read-only status register provides a summary of the chip status by indicating whether any diagnostic monitors have detected a fault and to determine the status of any programmed profile. The most significant three bits of the status register indicate critical system faults. The next two bits, bits 12 and 11, provide the status of the sequencer. Bits 10 to 7, 4, and 3 provide indicators for specific individual monitors and bits 2 and 1 are derived from the contents of the Diagnostic register.

The first most significant bit in the status register is the diagnostic status flag, FF. If any other fault bits in the status register are set, this bit is high. When STRn goes low, to start a serial transfer, SDO outputs the diagnostic status flag. This allows the main controller to poll the AMT49700 through the serial interface to determine if a fault has been detected. If no faults have been detected, then the serial transfer may be terminated without generating a serial read fault by ensuring that SCK remains high while STRn is low. When STRn goes high, the transfer will be terminated and SDO will go into its high-impedance state. The value of the FF bit can also be indicated by the level on the DIAG output. Note that the CA and SSA bits will not affect the value of the FF bit.

The second most significant bit (bit 14) is the POR bit. At power-up or after a power-on reset, the FF bit and the POR bit are set, indicating to the external controller that a power-on reset has taken place. All other diagnostic bits are reset and all other registers are returned to their default state. Note that a power-on reset only occurs when the outputs of the internal supply regulators (derived from VBB) rise to acceptable levels. Power-on reset is not directly affected by the state of the VBB supply or the charge pump output, VCP. In general, the UV bit will also be set following a power-on reset as the charge pump will not have reached its rising undervoltage threshold until after the register reset is completed.

The third bit in the status register (bit 13) is the SE bit, which indicates that the previous serial transfer (read or write) was not completed successfully.

Bit 12 is the CR (command ready) bit. CR is set to 1 when the AMT49700 is able to accept a new profile command. If a new profile command is input when CR is 0, then that command will be ignored. CR has no effect on the diagnostic status flag, FF.

Bit 11 is the SSA (step sequence active) bit. SSA is set to 1 when a programmed step sequence starts and is active and will be set to 0 when the step sequence completes and is inactive. SSA has no effect on the diagnostic status flag, FF. The value of the SSA bit can also be indicated by the level on the DIAG output by setting DSG[2:0] to [110].

Bits 10 to 3 contain fault bits for the eight individual monitors OT, TW, OV, UV, OLA, and OLB. If any of these faults remain following a Status register reset, then the corresponding bit will remain set. Resetting only affects latched fault bits for faults that are no longer present. For any static faults that are still present, for example overtemperature, the fault flag will remain set after the reset.

The remaining bits, OCB and OCA, are derived from the contents of the Diagnostic register.

The Diagnostic register is an additional read-only register that can be read with a normal serial register read sequence. This register contains additional fault information that permits specific identification of the affected drive MOSFET if an overcurrent fault is detected. If an attempt is made to write to the Diagnostic register, it will be ignored, no data will be written, and the remaining eleven bits output on SDO will be the least significant ten bits of the status register and a parity bit.

If any of the phase B overcurrent fault bits, BML, BMH, BPL, BPH, in the Diagnostic register are set OCB is set. If any of the phase A overcurrent fault bits, AML, AMH, APL, APH, in the Diagnostic register are set, OCA is set. OCB and OCA are not affected by clearing the Status register. They are only cleared when the corresponding contents of the Diagnostic register are cleared. If, upon reading the Status register, OCA or OCB is found to be set to 1, the Diagnostic register may be read to locate the source of the fault and clear the fault state.

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RESETTING STATUS AND DIAGNOSTIC REGISTERS

The Status and Diagnostic registers are cleared of latched faults and any static faults that are no longer present by any of four actions:

- Reading the register with DSR = 0.
- Performing a fault reset by pulsing the RESETn input low for the duration reset pulse with, t_{RST}, or by writing the RST bit to 1.
- Going through a sleep-wake cycle by holding RESETn low or writing the GTS bit to 1.
- Cycling the power off and on.

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SERIAL REGISTER REFERENCE

Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: PWM config	0	0	0	0	WR	PM4	PM3	PM2	PM1	PM0	PW4	PW3	PW2	PW1	PW0	P
					0	0	0	1	0	0	1	0	1	0	0	
1: PWM config	0	0	0	1	WR		DP2	DP1	DP0	DD1	DD0	DS3	DS2	DS1	DS0	P
					0	0	0	0	0	0	0	0	0	0	0	

Register 0: PWM Configuration

PM[4:0] Maximum PWM on time

$$t_{PMX} = t_{PW} \times (n \times 64\ \mu s)$$

where *n* is a positive integer defined by PM[4:0], t_{PW} is the PWM period (below),

e.g. when PM[4:0] = [00100], then $t_{PMX} = 256 \times t_{PW}$ µs.

The range of t_{PMX} is $64 \times t_{PW}$ to $1984 \times t_{PW}$ µs.

Setting PM[4:0] to 0 will disable checking of the maximum on-time.

PW[4:0] Bridge PWM Fixed Period

$$t_{PW} = 36\ \mu s + (n \times 0.8\ \mu s)$$

where *n* is a positive integer defined by PW[4:0], e.g. when PW[4:0] = [1 0100] then $t_{PW} = 52$ µs.

The range of t_{PW} is 36 to 60.8 µs.

This is equivalent to 27.8 to 16.4 kHz.

Register 1: PWM Configuration

DP[2:0] PWM Dither Step Period

$$t_{\Delta PW} = -0.2\ \mu s - (n \times 0.2\ \mu s)$$

where *n* is a positive integer defined by DP[2:0], e.g. when DP[2:0] = [101] then $t_{\Delta PW} = -1.2$ µs.

The range of $t_{\Delta PW}$ is –0.2 µs to –1.6 µs.

DD[1:0] PWM Dither Dwell Time

DD1	DD0	Dwell Time	Default
0	0	1 ms	D
0	1	2 ms	
1	0	5 ms	
1	1	10 ms	

DS[3:0] PWM Dither Step Count

The number of dither steps is directly defined by the integer value of DS[3:0], e.g. when DS[3:0] = [0111] then there will be 7 frequency steps.

The maximum number of steps is 15.

Setting DS[3:0] to 0 will disable PWM dither.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2: Current Config	0	0	1	0	WR	DIS	HLR	SLW	TBK1	TBK0	MXI4	MXI3	MXI2	MXI1	MXI0	P
					0	1	0	0	1	1	1	0	0	0	0	
3: Diagnostics Config	0	0	1	1	WR	DGS2	DGS1	DGS0		OLT	TOL1	TOL0	OFA	TOC1	TOC0	P
					0	0	0	0	0	0	1	0	0	0	1	

Register 2: Current Configuration

DIS Disable Bridge Output

DIS	Bridge Output	Default
0	Enabled	
1	Disabled	D

HLR Slow decay recirculation path

HLR	Recirculation Path	Default
0	High Side	D
1	Low Side	

SLW Slew Control

SLW	Bridge Slew Time	Default
0	Fast	D
1	Slow	

TBK[1:0] Current Compare Blank Time

TBK1	TBK0	Blank time	Default
0	0	1.0 µs	
0	1	1.5 µs	
1	0	2.5 µs	
1	1	3.5 µs	D

MXI[4:0] Maximum Phase Current

$$I_{MX} = (n + 1) \times 50\ mA$$

where n is a positive integer defined by MXI[4:0]

e.g. when MXI[4:0] = [1 0000] then I_{MX} = 850 mA

The range of I_{MX} is 50 mA to 1600 mA.

Register 3: Diagnostics Configuration

DGS[2:0] DIAG output select

DGS2	DGS1	DGS0	DIAG output	Default
0	0	0	General fault, active low	D
0	0	1	Supply fault, active low	
0	1	0	Open load, active low	
0	1	1	Temperature as voltage	
1	0	0	PWMA output	
1	0	1	STEP Signal	
1	1	0	Motion Control, active low	
1	1	1	Clock (/256000)	

OLT Open Load Threshold

OLT	Open Load Threshold	Default
0	13 mA	D
1	26 mA	

TOL[1:0] Open Load Detect Time

TOL1	TOL0	OL Detect Time	Default
0	0	10 ms	
0	1	20 ms	
1	0	30 ms	D
1	1	40 ms	

OFA Overcurrent Fault Action

OFA	Overcurrent Fault Action	Default
0	Retry	D
1	Disable outputs	

TOC[1:0] Overcurrent fault delay

TOC1	TOC0	Detect delay time	Default
0	0	1 µs	
0	1	2 µs	D
1	0	3 µs	
1	1	4 µs	

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
5: Single Step Control	0	1	0	1	WR	SAR				SC5	SC4	SC3	SC2	SC1	SC0	P
					0	0	0	0	0	0	0	0	0	0	0	
6: System control	0	1	1	0	WR	GTS	RST	VLR	MS2	MS1	MS0	DSR	BRK	END	STP	P
					0	0	0	0	0	1	0	0	0	0	0	

Register 5: Single Step Control

SAR Step Angle Reset

SAR	Phase Outputs	Default
0	Normal operation	D
1	Reset to home position	

HLR Step change number.
2's complement format.
Positive value increases step angle number.
Negative value decreases step angle number.

Register 6: System Control

GTS Go to sleep command

GTS	Sleep transition	Default
0	No change in state	D
1	No change in state	
1 → 0	No change in state	
0 → 1	Enter sleep state	

RST Reset Faults

RST	Fault Reset Action	Default
0	No action	D
1	No Action	
0 → 1	Reset faults	
1 → 0	No Action	

VLR Logic I/O voltage select

VLR	Logic I/O Voltage	Default
0	3.3 V	D
1	5 V	

Register 6: System Control (continued)

MS[2:0] Microstep resolution

MS2	MS1	MS0	Microstep Resolution	Default
0	0	0	Full Two Phase	
0	0	1	Full One Phase Detent	
0	1	0	1/2 Compensated	D
0	1	1	1/2 Uncompensated	
1	0	0	1/4	
1	0	1	1/8	
1	1	0	1/16	
1	1	1	1/16	

DSR Disable Serial Reset

DSR	Brake Action	Default
0	Enable Serial Reset	D
1	Disable Serial Reset	

BRK Brake command

BRK	Brake Action	Default
0	No Brake	D
1	Brake Applied	

END End Sequence Command

END	Effect on sequence	Default
0	No effect	D
1	Decelerate and halt	

STP Stop Sequence Command

STP	Effect on sequence	Default
0	No Effect	D
1	Immediately halt	

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7: Step Count (lsb)	0	1	1	1	WR	DIR	CRM	NSL7	NSL6	NSL5	NSL4	NSL3	NSL2	NSL1	NSL0	P
					0	0	0	0	0	0	0	0	0	0	0	
8: Step Count (msb)	1	0	0	0	WR			NSM7	NSM6	NSM5	NSM4	NSM3	NSM2	NSM1	NSM0	P
					0	0	0	0	0	0	0	0	0	0	0	
9: Acceleration	1	0	0	1	WR					ACC5	ACC4	ACC3	ACC2	ACC1	ACC0	P
					0	0	0	0	0	0	0	0	0	0	0	
10: Deceleration	1	0	1	0	WR					DEC5	DEC4	DEC3	DEC2	DEC1	DEC0	P
					0	0	0	0	0	0	0	0	0	0	0	

Register 7: Step Count

DIR Motor stepping Direction

DIR	Step Direction	Default
0	Forward	D
1	Reverse	

NSL[7:0] Least significant 8 bits of the number of steps to take in a sequence.

CRM Continuous Run Mode

CRM	Run Mode	Default
0	Profile or Step Command	D
1	Continuous	

Register 8: Step Count

NSM[7:0] Most significant 8 bits of the number of steps to take in a sequence.

Register 9: Acceleration

ACC[5:0] Acceleration Setting

$$a = n \times 65\ Full\ step / s^2$$

where n is a positive integer defined by ACC[7:0],
a is the acceleration in Step/s^2,
e.g., when ACC[5:0] = [01 1000]
then a = 1560 Fullstep/s^2.

The range of a is 0 to 4095 Fullstep/s^2.

Register 10: Deceleration

DEC[5:0] Deceleration Setting

$$a = -n \times 65\ Full\ step / s^2$$

where n is a positive integer defined by DEC[7:0],
a is the acceleration in Full Step/s^2,
e.g., when DEC[5:0] = [01 1000]
then a = –1560 Fullstep/s^2.

The range of a is 0 to –4095 Fullstep/s^2.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11: Min Step Rate	1	0	1	1	WR					SSR5	SSR4	SSR3	SSR2	SSR1	SSR0	P
					0	0	0	0	0	0	0	0	0	0	0	
12: Max Step Rate	1	1	0	0	WR					RSR5	RSR4	RSR3	RSR2	RSR1	RSR0	P
					0	0	0	0	0	0	0	0	0	0	0	
13: STEP Readback	1	1	0	1	R	DIRR				SA5	SA4	SA3	SA2	SA1	SA0	P
					0	0	0	0	0	0	0	0	0	0	0	

Register 11: Starting Step Rate

SSR[5:0] Starting Step Rate in Full Step/s

$$R_{STT} = (n + 1) \times 2 \text{ Full step/s}$$

Register 12: Running Step Rate

RSR[5:0] Running Step Rate in Full Step/s

$$R_{RUN} = (n + 1) \times 16 \text{ Full step/s}$$

For both SSR and RSR, the step rate is in full steps/s. This is maintained for all microstep resolutions. The number of microsteps per second is a multiple of the programmed step rate based on the number of microsteps per full step.

Register 13: STEP Readback

DIRR STEP direction readback

SA[5:0] Step Angle Number readback

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
14: Mask	1	1	1	0	WR	OT	TW	OV	UV			OLB	OLA	OCB	OCA	P
					0	0	0	0	0	0	0	0	0	0	0	
15: Diagnostic	1	1	1	1	WR			BML	BMH	BPL	BPH	AML	AMH	APL	APH	P
						0	0	0	0	0	0	0	0	0	0	
Status	FF	POR	SE	CR	SSA	OT	TW	OV	UV			OLB	OLA	OCB	OCA	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

Register 14: Mask register

OT Overtemperature
TW Temperature Warning
OV VBB Overvoltage
UV Undervoltage on VBB or VCP
OLB Phase B open load
OLA Phase A open load
OCB Phase B overcurrent
OCA Phase A overcurrent

xx	Fault mask	Default
0	Fault detection permitted	D
1	Fault detection disabled	

Register 15: Diagnostic

BML Overcurrent on BM Output low-side
BMH Overcurrent on BM Output high-side
BPL Overcurrent on BP Output low-side
BPH Overcurrent on BP Output high-side
AML Overcurrent on AM Output low-side
AMH Overcurrent on AM Output high-side
APL Overcurrent on AP Output low-side
APH Overcurrent on AP output high-side

Status Register

FF Status Flag
POR Power-on-reset
SE Serial Error
CR Command Ready for Motion Profile
SSA Step Sequence Active indicator
OT Overtemperature
TW Temperature warning
OV Overvoltage on VBB
UV Undervoltage on VBB or VCP
OLB Open load on phase B
OLA Open load on phase A
OCB Overcurrent on phase B
OCA Overcurrent on phase A

xx	Fault	Default
0	No fault detected	D
1	Fault detected	

Status Register bit map to Diagnostic Register

Status Register Bit	Related Diagnostic Register Bits
OCB	BML, BMH, BPL, BPH
OCA	AML, AMH, APL, APH

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Table 3: Phase Current Table [1][2] (default, power-on content)

Step Number					Phase Current [%I_{SMAX}]		Step Angle	Phase		DAC	
Full	1/2	1/4	1/8	1/16	A	B		A	B	A	B
	0	0	0	0	0.00%	100.00%	0.0	0	0	0	63
				1	9.38%	100.00%	5.4	0	0	5	63
			1	2	18.75%	98.44%	10.8	0	0	11	62
				3	29.69%	95.31%	17.3	0	0	18	60
		1	2	4	37.50%	92.19%	22.1	0	0	23	58
				5	46.88%	87.50%	28.2	0	0	29	55
			3	6	56.25%	82.81%	34.2	0	0	35	52
				7	64.06%	76.56%	39.9	0	0	40	48
0	1	2	4	8	70.31%	70.31%	45.0	0	0	44	44
				9	76.56%	64.06%	50.1	0	0	48	40
			5	10	82.81%	56.25%	55.8	0	0	52	35
				11	87.50%	46.88%	61.8	0	0	55	29
		3	6	12	92.19%	37.50%	67.9	0	0	58	23
				13	95.31%	29.69%	72.7	0	0	60	18
			7	14	98.44%	18.75%	79.2	0	0	62	11
				15	100.00%	9.38%	84.6	0	0	63	5
	2	4	8	16	100.00%	0.00%	90.0	0	0	63	0
				17	100.00%	–9.38%	95.4	0	1	63	5
			9	18	98.44%	–18.75%	100.8	0	1	62	11
				19	95.31%	–29.69%	107.3	0	1	60	18
		5	10	20	92.19%	–37.50%	112.1	0	1	58	23
				21	87.50%	–46.88%	118.2	0	1	55	29
			11	22	82.81%	–56.25%	124.2	0	1	52	35
				23	76.56%	–64.06%	129.9	0	1	48	40
1	3	6	12	24	70.31%	–70.31%	135.0	0	1	44	44
				25	64.06%	–76.56%	140.1	0	1	40	48
			13	26	56.25%	–82.81%	145.8	0	1	35	52
				27	46.88%	–87.50%	151.8	0	1	29	55
		7	14	28	37.50%	–92.19%	157.9	0	1	23	58
				29	29.69%	–95.31%	162.7	0	1	18	60
			15	30	18.75%	–98.44%	169.2	0	1	11	62
				31	9.38%	–100.00%	174.6	0	1	5	63
	4	8	16	32	0.00%	–100.00%	180.0	0	1	0	63

Step Number					Phase Current [%I_{SMAX}]		Step Angle	Phase		DAC	
Full	1/2	1/4	1/8	1/16	A	B		A	B	A	B
	4	8	16	32	0.00%	–100.00%	180.0	0	1	0	63
				33	–9.38%	–100.00%	185.4	1	1	5	63
			17	34	–18.75%	–98.44%	190.8	1	1	11	62
				35	–29.69%	–95.31%	197.3	1	1	18	60
		9	18	36	–37.50%	–92.19%	202.1	1	1	23	58
				37	–46.88%	–87.50%	208.2	1	1	29	55
			19	38	–56.25%	–82.81%	214.2	1	1	35	52
				39	–64.06%	–76.56%	219.9	1	1	40	48
2	5	10	20	40	–70.31%	–70.31%	225.0	1	1	44	44
				41	–76.56%	–64.06%	230.1	1	1	48	40
			21	42	–82.81%	–56.25%	235.8	1	1	52	35
				43	–87.50%	–46.88%	241.8	1	1	55	29
		11	22	44	–92.19%	–37.50%	247.9	1	1	58	23
				45	–95.31%	–29.69%	252.7	1	1	60	18
			23	46	–98.44%	–18.75%	259.2	1	1	62	11
				47	–100.00%	–9.38%	264.6	1	1	63	5
	6	12	24	48	–100.00%	0.00%	270.0	1	1	63	0
				49	–100.00%	9.38%	275.4	1	0	63	5
			25	50	–98.44%	18.75%	280.8	1	0	62	11
				51	–95.31%	29.69%	287.3	1	0	60	18
		13	26	52	–92.19%	37.50%	292.1	1	0	58	23
				53	–87.50%	46.88%	298.2	1	0	55	29
			27	54	–82.81%	56.25%	304.2	1	0	52	35
				55	–76.56%	64.06%	309.9	1	0	48	40
3	7	14	28	56	–70.31%	70.31%	315.0	1	0	44	44
				57	–64.06%	76.56%	320.1	1	0	40	48
			29	58	–56.25%	82.81%	325.8	1	0	35	52
				59	–46.88%	87.50%	331.8	1	0	29	55
		15	30	60	–37.50%	92.19%	337.9	1	0	23	58
				61	–29.69%	95.31%	342.7	1	0	18	60
			31	62	–18.75%	98.44%	349.2	1	0	11	62
				63	–9.38%	100.00%	354.6	1	0	5	63
	0	0	0	0	0.00%	100.00%	0.0	0	0	0	63

[1] To be read in conjunction with Table 6: Step Angle Allocation
[2] The home position is defined as step number 8 for all modes of operation except 1-phase full step in which home is defined as step 0

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APPLICATIONS INFORMATION

Motor Microstepping

The key to understanding microstepping lies in understanding the phase current table. This table contains the relative phase current magnitude and direction for each of the two motor phases at each microstep position. The maximum resolution of the AMT49700 is 1/16th microstep—that is, 16 microsteps per full step. There are 4 full steps per electrical cycle so the phase current table has 64 microstep entries. The entries are numbered from 0 to 63. This number represents the phase angle within the full 360° electrical cycle and is called the step angle number. This is illustrated in Figure 8.

PHASE TABLE AND PHASE DIAGRAM

Figure 8 shows the contents of the phase current table as a phase diagram. The phase B current, I_B, from the phase current table, is plotted on horizontal axis and the phase A current, I_A, is plotted on the vertical axis. The resultant motor current at each microstep is shown as numbered radial arrows. The number shown corresponds to the 1/16th microstep step angle number in the phase current table.

Figure 7 shows an example of calculating the resultant motor current magnitude and angle for step number 28. The target is to have the magnitude of the resultant motor current to be 100% at all microstep positions. The relative phase currents from the phase current table are:

$$I_A = 37.50\%$$

$$I_B = -92.19\%$$

Assuming a full-scale (100%) current of 1 A means that the two phase currents are:

$$I_A = 0.3750\ A$$

$$I_B = -0.9219\ A$$

The magnitude of the resultant will be the square root of the sum of the squares of these two currents:

$$|I_{28}| = \sqrt{I_A^2 + I_B^2} = \sqrt{0.1406 + 0.8499} = 0.9953 \qquad (A)$$

So the resultant current magnitude is 99.53% of full scale. This is within 0.5% of the target 100% and is well within the ±10% accuracy of the AMT49700.

The reference angle, that is zero degrees (0°), within the full electrical cycle (360°), is defined as the angle where I_B is at +100% and I_A is zero. Each full step is represented by 90° in the electrical cycle, so each 1/16th microstep is (90°/16 steps =) 5.625°.

The target angle of each microstep position with the electrical cycle is determined by product of the step angle number and the angle for a single microstep. So for the example of Figure 7:

$$\alpha_{28(TARGET)} = 28 \times 5.625^o = 157.5^o$$

The actual angle is calculated using basic trigonometry as:

$$\alpha_{28(ACTUAL)} = 180 + \tan\text{-}1\left(\frac{I_{A28}}{I_{B28}}\right) = 180 + (-22.1) = 157.9^o$$

So the angle error is only 0.4°. Equivalent to about 0.1% error in 360° and well within the current accuracy of the AMT49700.

Note that each phase current in the AMT49700 is defined by a 6-bit DAC. This means that the smallest resolution of the DAC is 100 / 64 = 1.56% of the full scale, so the AMT49700 cannot produce a resultant motor current of exactly 100% at each microstep, nor can it produce an exact microstep angle. However, as can be seen from the calculations above, the results for both are well within the specified accuracy of the AMT49700 current control. The resultant motor current angle and magnitude are also more than precise enough for all but the highest precision stepper motors.

With the phase table, control of a stepper motor is simply a matter of increasing or reducing the step angle number to move round the phase diagram of Figure 8. This can be in predefined multiples using the step sequencer or it can be variable using the direct single step control.

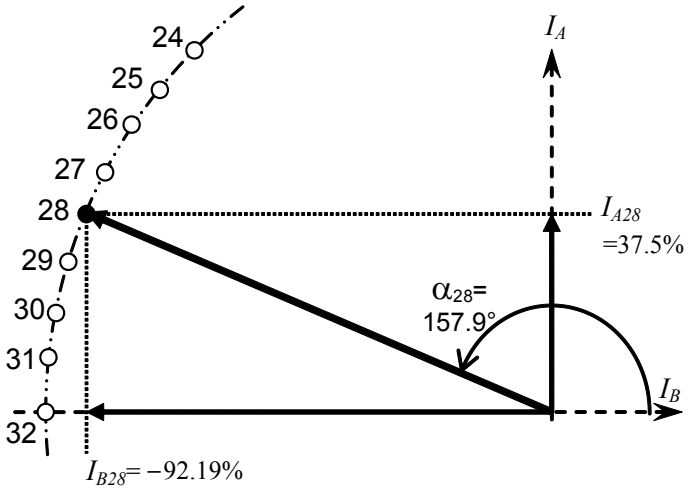

Figure 7: Calculating the Resultant Motor Current

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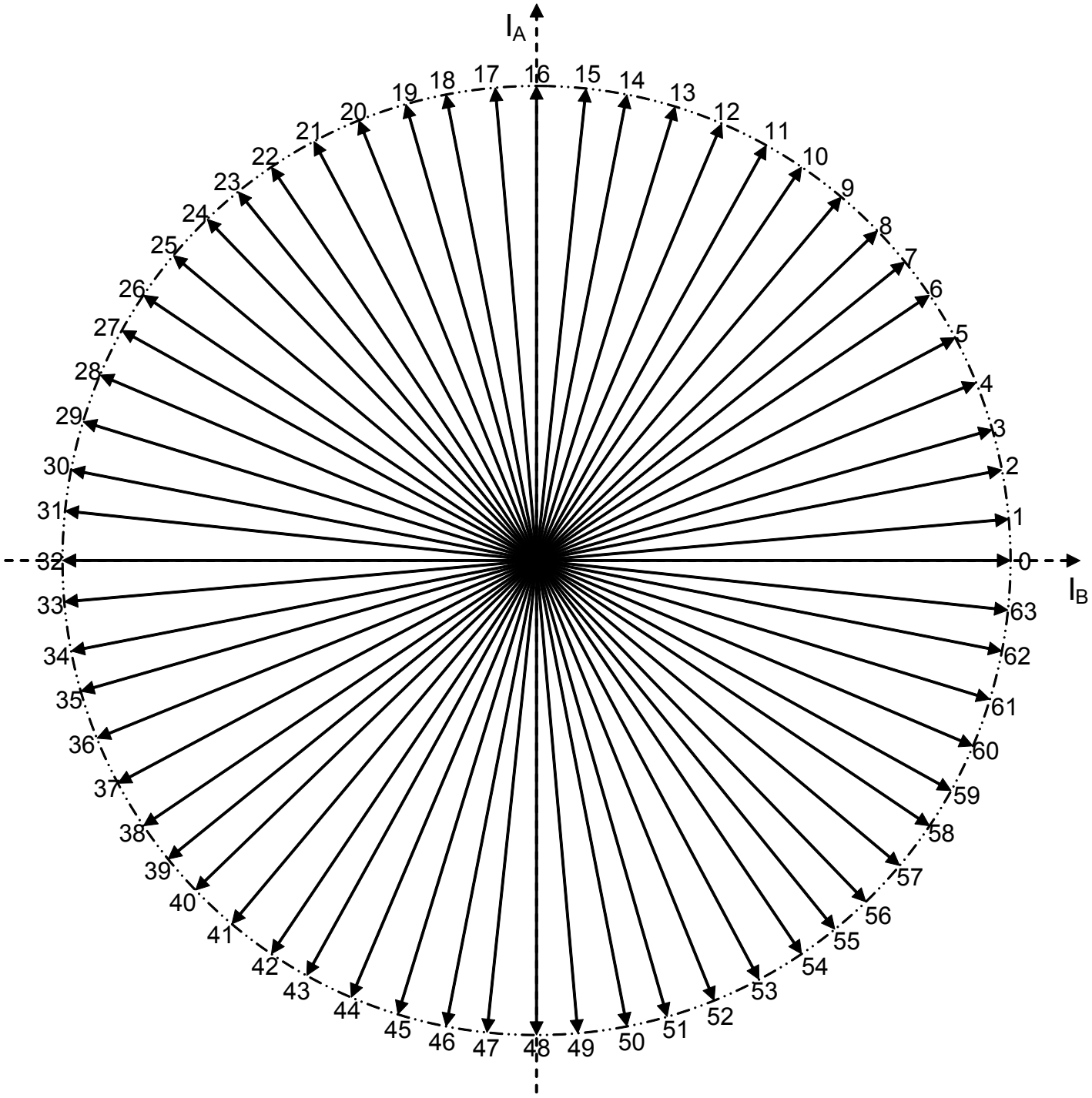

Figure 8: Phase Current Table as a Phase Diagram

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MICROSTEPPING WITH THE STEP SEQUENCER

When using the programmable step sequence control method, the step sequencer provides a step command at the appropriate time to move the motor at the microstep resolution defined by the MS[2:0] bits. The DIR input defines the motor direction. These inputs define the output of a step angle counter that determines the required step angle number in the phase current table. Table 3 summarizes the step angle numbers used for the resolutions available when using the step sequencer to control the output of the AMT49700.

In sixteenth step mode, the step angle counter simply increments or decrements the step angle number by one on each rising edge of the step input depending on the logic state of the DIR input. In the other microstep resolution modes, the step angle counter outputs specific step angle numbers as defined in the phase current table, Table 3, and summarized in Table 4.

Table 4: Step Angle Allocation

Mode	Step angle numbers used
Full 1 phase	0, 16, 32, 48
Full 2 phase	8, 24, 40, 56
Half Compensated.	0, 8, 16, 24, 32, 40, 48,56
Half Uncompensated	0, 0/16, 16, 16/32, 32, 32/48, 48, 48/0
Quarter	0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, 60
Eighth	0, 2, 4, 6, 8, 10, 12, 14, 16 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52, 54, 56, 58, 60, 62
Sixteenth	All

There are two full-step modes available: 1-phase and 2-phase. In both cases, four of the entries in the phase current table are used.

1-phase full-step mode uses step angles 0, 16, 32, and 48, as shown in Figure 9, and only one phase is active at any time. These step angles place the motor at the detent points, the positions where the motor naturally settles to minimize the internal magnetic path reluctance. This mode has the advantage that once the motor movement has stopped, the current can be reduced to a very low level to hold the motor. The magnetic fields will be acting with any hold current to prevent motor movement.

2-phase mode uses step angles 8, 24, 40, and 56 as shown in Figure 10. In this case, two phases are always active at each step position. There are two advantages in using these positions rather than the single full current positions. With both phases active, the power dissipation is shared between two drivers. This slightly improves the ability to dissipate the heat generated and reduces the stress on each driver. The second advantage is that the holding torque can be more effective because the forces holding the motor are mainly rotational rather than mainly radial.

Two half-step modes are available: compensated and uncompensated. Compensated mode uses eight of the entries in the phase current table. These are 0, 8, 16, 24, 32, 40, 48, and 56 as shown in Figure 11. In this mode, the current in each phase is compensated for the step angle to ensure that the average torque is the same at all step positions.

Uncompensated half-step mode does not reduce the current based on the step angle. Instead, each phase is driven to the current target defined by the 100% current value at steps 0, 16, 32, or 48 in the phase angle table. The current polarity is the same at each half step angle as defined in the phase angle table. The resulting phase diagram is shown in Figure 12.

Quarter step uses sixteen of the entries in the phase current table. These are the multiples of 4, namely 0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, and 60 as shown in Figure 13. Eighth-step mode uses the 32 even-numbered entries in the phase current table including 0, namely 0, 2, 4, and so on, up to 58, 60, and 62 as shown in Figure 14.

In quarter-step, eighth-step, and sixteenth step modes, the current in each phase is compensated for the step angle to ensure that the average torque is the same at all step positions.

The microstep selection can be changed between step commands from the step sequencer. When the microstep resolution changes, the AMT49700 moves to the next available step angle number at the new resolution on the next rising edge of the STEP input. For example, if the microstep mode is sixteenth and the present step angle is 57, then with the direction forwards (increasing step angle), changing to quarter-step mode will cause the phase number to go to 60 on the next rising edge of the STEP input, changing to half-step mode will cause the phase number to go to 0 on the next rising edge of the STEP input.

On first power-up, after a power-on reset or after sleep, the step angle number is set to 8, equivalent to the electrical 45° position, except for full-step single phase drive where the step angle number is set to 0. This position is defined as the “home” position.

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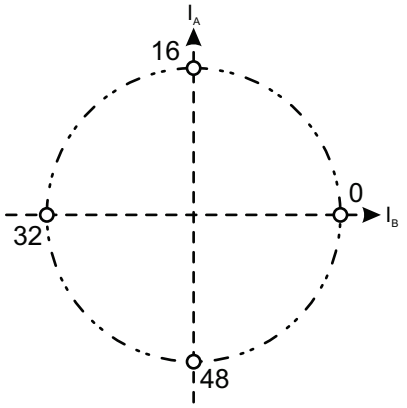

Figure 9: Full-Step 1-Phase Drive Phase Diagram

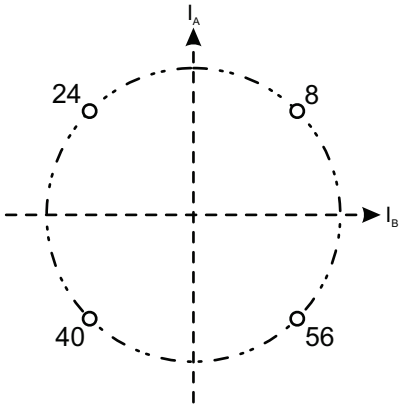

Figure 10: Full-Step 2-Phase Drive Phase Diagram

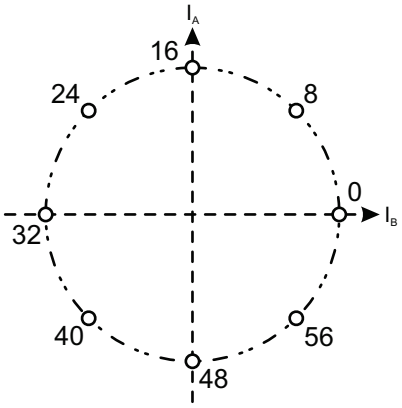

Figure 11: Compensated Half-Step Phase Diagram

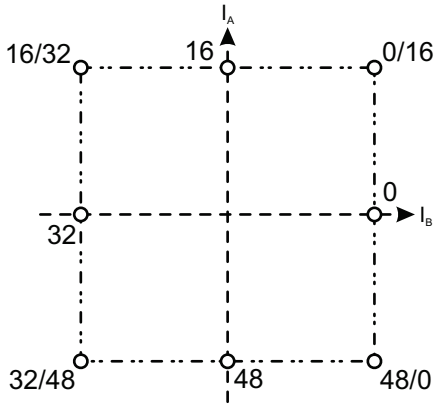

Figure 12: Uncompensated Half-Step Phase Diagram

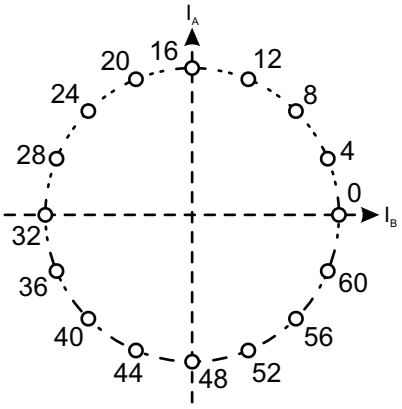

Figure 13: Quarter-Step Phase Diagram

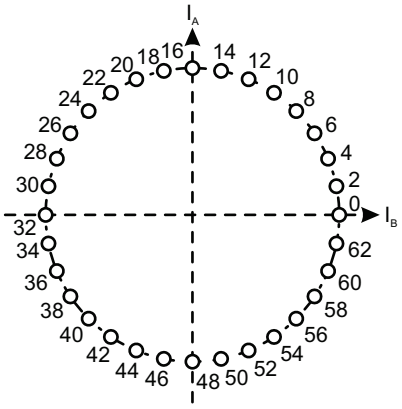

Figure 14: Eighth-Step Phase Diagram

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SINGLE-STEP CONTROL

The motor movement can be controlled one step at a time through the serial interface by directly increasing or decreasing the step angle number. The maximum value of the step angle number is 63 and the minimum number is 0. Therefore, any increase or reduction in the microstep number is performed using modulo 64 arithmetic. This means that increasing a step angle number of 63 by 1 will produce a step angle number of 0, increasing by two from 63 will produce 1, and so on. Similarly, in the reverse direction, reducing a step angle number of 0 by 1 will produce a step angle number of 63, decreasing by two from 0 will produce 62, and so on.

The step angle is changed by writing a value to the SC[5:0] variable. This number is a two's complement number that is added to the step angle number causing it to increase or decrease. Two's complement is the natural integer number system for most microcontrollers. This allows standard arithmetic operators to be used, within the microcontroller, to determine the size of the next step increment. Table 5 shows, for clarity, the binary equivalent of each decimal number between 16 and +16.

Each increase in the step angle number represents a forwards movement of one-sixteenth microstep. Each decrease in the step angle number represents a reverse movement of one-sixteenth microstep.

To move the motor one full step, the step angle number must be increased or reduced by 16. To move the motor one half step, the step angle number must be increased or reduced by 8. For one quarter step, the step angle number must be increased or reduced by 4. And for one eighth step, the step angle number must be increased or reduced by 2.

For example, to continuously move the motor forwards in quarter step increments, the number 4 (00 0100) is repeatedly written to SC[5:0] through the serial interface (see Figure 15). To move the motor backwards in quarter step increments, the number –4 (11 1100) is repeatedly written to SC[5:0] (see Figure 17). Figure 17 and Figure 18 show half-step forwards and eighth-step backwards sequences, respectively.

Table 5: Two's Complements

Decimals	2's Comp.	Decimals	2's Comp.
0	00 0000		
1	00 0001	–1	11 1111
2	00 0010	–2	11 1110
3	00 0011	–3	11 1101
4	00 0100	–4	11 1100
5	00 0101	–5	11 1011
6	00 0110	–6	11 1010
7	00 0111	–7	11 1001
8	00 1000	–8	11 1000
9	00 1001	–9	11 0111
10	00 1010	–10	11 0110
11	00 1011	–11	11 0101
12	00 1100	–12	11 0100
13	00 1101	–13	11 0011
14	00 1110	–14	11 0010
15	00 1111	–15	11 0001
16	01 0000	–16	11 0000

With this control mode, the step rate is controlled by the timing of the serial interface and is the inverse of the step time, t_{STEP}, shown in Figure 15. The motor step only takes place when the STRn goes from low to high when writing the value into SC[5:0]. The motor step rate is therefore determined by the timing of the rising edge of the STRn input. The clock rate of the serial interface, defined by the frequency of the SCK input, has no direct effect on the step rate.

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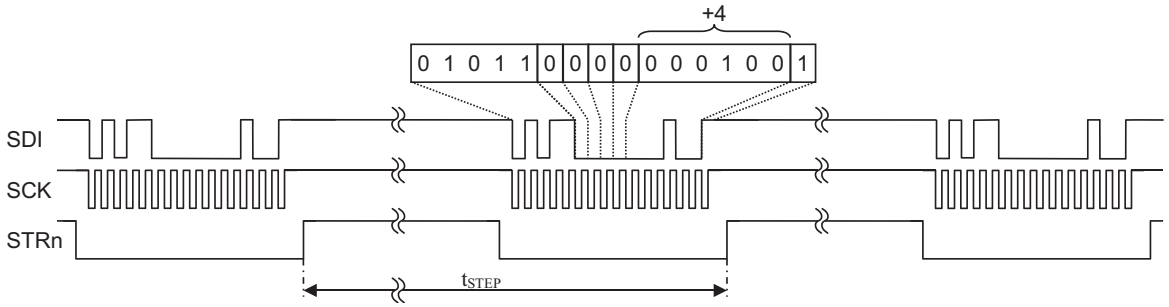

Figure 15: Serial Interface Sequence for Quarter Step in Forward Direction

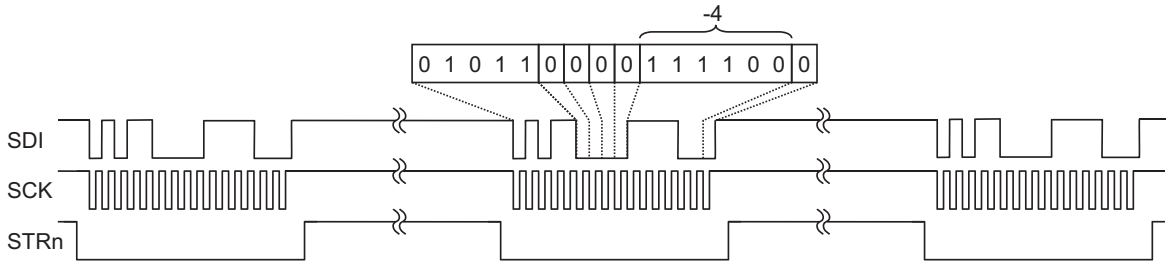

Figure 16: Serial Interface Sequence for Quarter Step in Reverse Direction

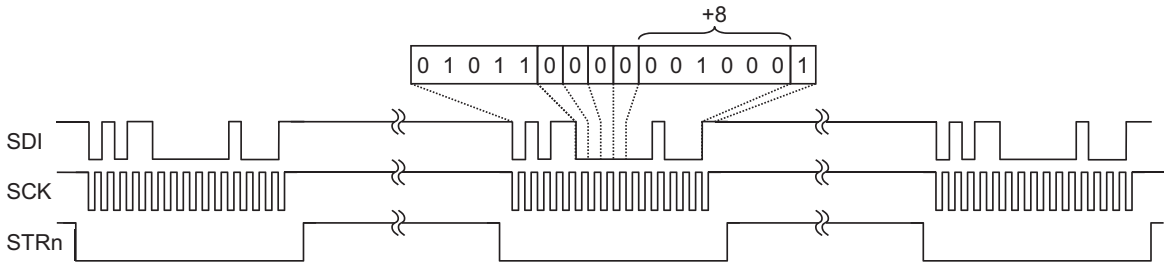

Figure 17: Serial Interface Sequence for Half Step in Forward Direction

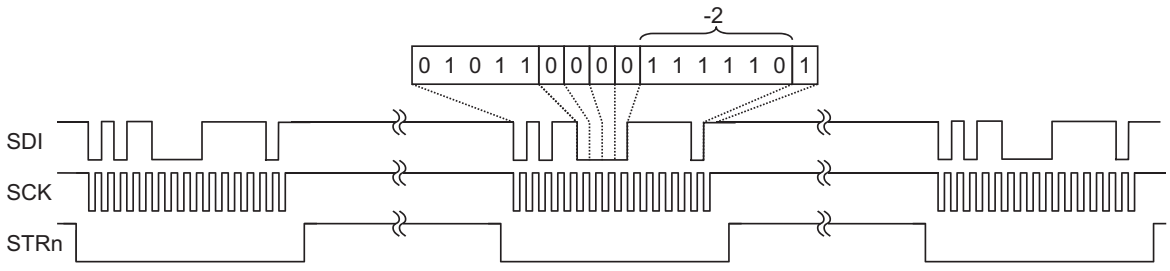

Figure 18: Serial Interface Sequence for Eighth Step in Reverse Direction

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Motion Control with the Step Sequencer

The basic operation of the programmable step sequencer is described in the "Stepper Motor Motion Control" section. The motion is described by 5 programmable variables, giving the start step rate, run step rate, acceleration, deceleration, and the total number of steps to take. These are illustrated in Figure 5, repeated here.

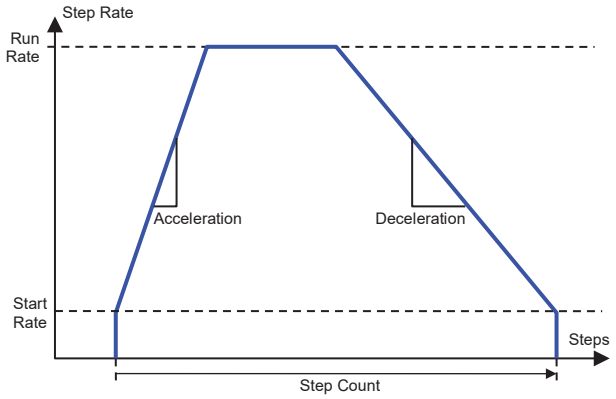

Figure 5: Step Profile Parameters

In the normal single sequence from a stationary state shown in Figure 5, the sequencer will begin by stepping the motor at the programmed start rate for the first step. The following steps will increase in step rate according to the programmed acceleration until the motor reaches the run step rate. At each step, the total step count remaining is reduced by one. The motor continues to be stepped at the run step rate until the step count reaches the number of steps required to decelerate the motor, based on the present step rate, the start rate, and the deceleration factor. At this point, the step rate is reduced at each step according to the programmed deceleration until the motor reaches the start step rate at the step count. Once the step count is reached the motor is stopped.

If the number of steps is insufficient to accelerate to the full run speed, the sequencer will accelerate the motor until it reaches the number of steps required to decelerate the motor for the present speed and will then change immediately to deceleration as shown in Figure 19. The motor will then continue to decelerate until the motor reaches the step count.

A single sequence is relatively simple to comprehend, but it is also possible to change the variables when a step sequence in in progress. A sequence can only start or be changed on the rising edge of the STRn input following the writing of the least significant 8 bits of the step count variable, NSL (the serial interface timing sequence is shown in Figure 2). Any changes to the start or run speed settings, the acceleration, deceleration, or the most significant 8 bits of the step count variable will have no effect until the least significant 8 bits of the step count variable are succesfully written.

If a change occurs when the sequence is in progress, the step sequencer will either continue running at the run step rate, accelerate the motor or decelerate the motor (Figure 20). The step count will be updated with the new step count. If there is no change to the most significant 8 bits of the step count, then the previous value will be retained and only the least significant 8 bits will be changed. If only the step rate is changed, then the least significant 8 bits of the step count should be written with the same value as the original programmed input.

There are many profile change combinations possible. The following examples provide the response to specific changes as examples from which it should be possible to extrapolate other possible responses.

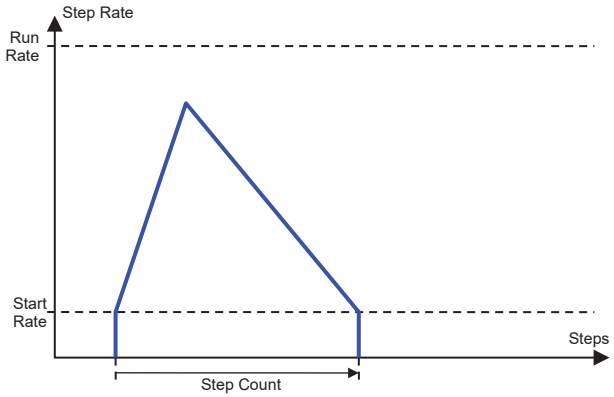

Figure 19: Low Step Count

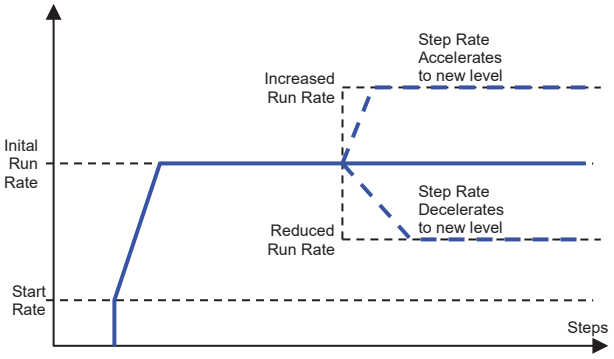

Figure 20: Run Speed Change

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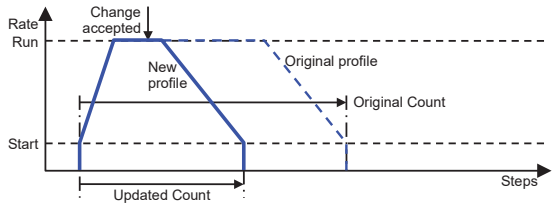

Figure 21a: Count Decrease (in time)

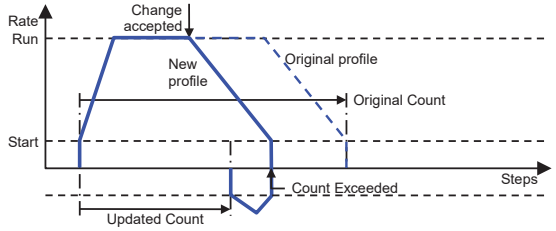

Figure 21b: Count Decrease (in time)

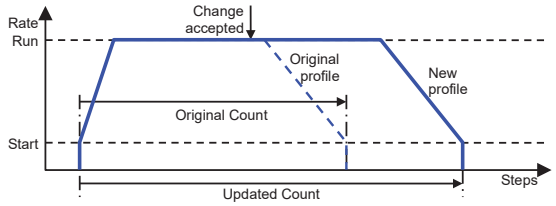

Figure 22a: Count Increase (in time)

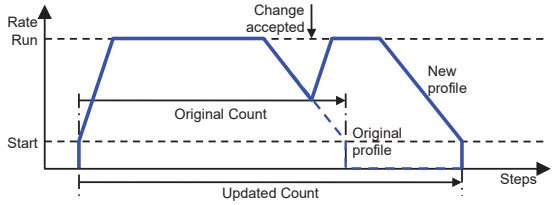

Figure 22b: Count Decrease (late)

If the step count is changed while a step sequence is in progress, the AMT49700 will immediately update the target count on the rising edge of the STRn input following the writing of the least significant 8 bits of the step count variable, NSL. The target count will still be relative to the starting position of the original step sequence command.

If an update results in a reduced step count and there is still sufficient time to continue stepping at the run rate (in time change) then the sequence will complete normally as shown in Figure 21a.

If an update results in a reduced step count and there is insufficient time to decelerate the motor to the new step count end point (late change), then deceleration will start immediately. The motor will continue to decelerate until it is running at the start step rate where it will stop. At this point the target count will be exceeded and the motor will be stepped in the reverse direction until it reaches the updated count position as shown in Figure 21b. The profile applied in the reverse direction will use the same acceleration, run rate, and deceleration parameters as in the forward direction.

If an update results in an increased step count and the motor is stepping at the run rate (in time change), then the sequence will complete normally as shown in Figure 22a.

If an update results in an increased step count and motor is decelerating (late change), then the motor will immediately start to accelerate at the programmed rate and follow the normal profile sequence as shown in Figure 22b.

If an update results in a change of direction, with or without a step count change, then the motor will immediately start to decelerate to a stop, then start a normal profile sequence in reverse, up to the new step count in the reverse direction. The step count is still relative to the original start point of the sequence as shown in Figure 23.

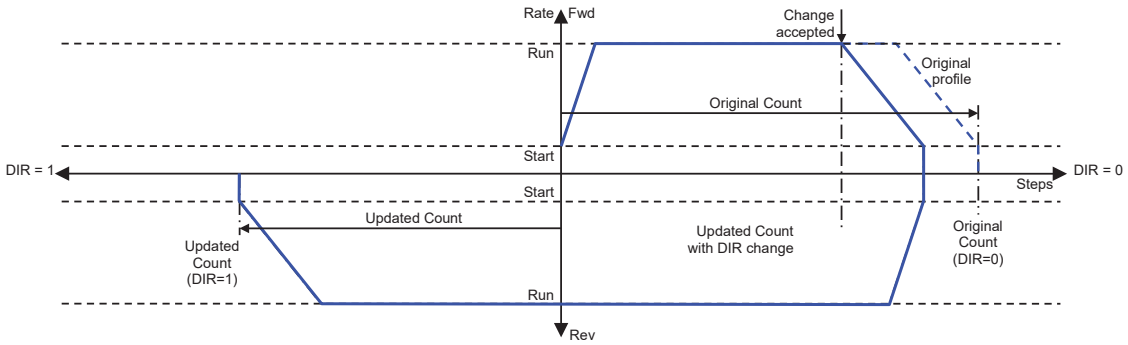

Figure 23: Direction Change

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PROFILE COMMAND UPDATE

When a new motion profile is input while a motion profile is in progress, the AMT49700 will update the target position relative to the existing start position from the previous command. If the previous motion profile has successfully completed, then any new motion profile will start from present position.

The status of the motion profile can be determined by reading the SSA bit in the Status register. The DIAG output can also be programmed to be low when SSA is set to 1.

A Command Ready bit, CR, is provided in the Status Register. If the CR bit is 1 when STRn goes low, then the AMT49700 will accept a new step sequence command. If the CR bit is 0 when STRn goes low, then the AMT49700 will not accept a new step sequence command. CR can be read out at the same time as Config 7 is being written. If CR = 1, the NSL command is accepted and then step sequence will start on the rising edge of STRn.

If a new command is inserted while CR is 0, then the AMT49700 will ignore the command.

CONTINUOUS RUN MODE

The AMT49700 has a function to continue stepping without the step number control. When the continuous run mode is active, the stepper motor will accelerate and run regardless of step demand until a stop command is inserted. This function allows to have a simple rotation application.

The Acceleration rate, ACC[5:0], Deceleration rate, DEC[5:0], Stating Step Rate, SSR[5:0], Running Step Rate, RSR[5:0], will be respected. The CRM bit in Configuration register 7 is used to activate the continuous run mode. When the CRM is set to 1, then continuous run mode will be active. The ACC, DEC, SSR, and RSR need to be preprogramed to reflect these ratios before sending the CRM. When the CRM is set to 1, these motion profile settings value will be taken in account. If the CRM bit set from 1 to 0, then the motion profile will decelerate and stop the motor.

The continuous run mode can accept motion profile parameters changing while in operation. The new motion profile parameters will be taken into account after transferring configuration register 7. When the motion profile is in deceleration to move to a new running step rate, if the same command is updated twice, deceleration will be skipped to run at the new running step rate.

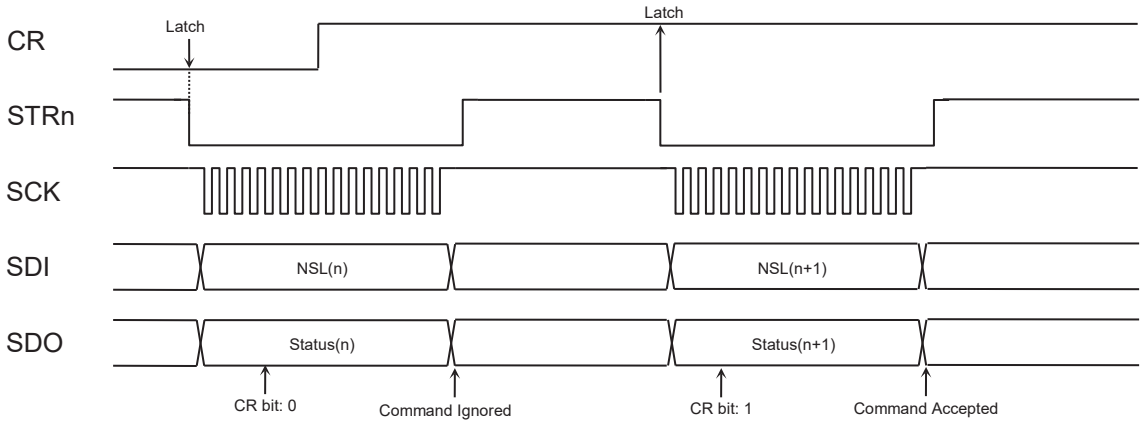

Figure 24: Motion Profile Update with CR Status Checking

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Layout

The printed wiring board (PWB) should use a higher weight copper thickness than a standard small signal or digital board. This helps to reduce the track impedance when conducting high currents. PWB traces carrying switching currents (i.e. power, ground, and bridge outputs) should be as wide and short as possible to minimize their inductance. This will help reduce any voltage transients caused by current switching during PWM current control.

For optimum thermal performance, the exposed thermal pad on the underside of the AMT49700 should be soldered directly onto the board. A solid ground plane should be added to the opposite side of the board and multiple vias through the board placed in the area under the thermal pad.

DECOUPLING

The power supply should be decoupled with an electrolytic capacitor in parallel with a ceramic capacitor. The ceramic capacitor should have a value of 100 nF and be placed as close as possible to the VBB and GND terminals of the AMT49700. The electrolytic capacitor should be rated to at least 1.5 times the intended maximum operating voltage and selected to support the maximum motor ripple current over the full system operating temperature range. (In many instances, actual capacitance value will be of secondary importance and device selection will be driven by ripple current rating and ESR.) This device should also be located close to the AMT49700.

The pump capacitor between CP1 and CP2 and the pump storage capacitor between VCP and VBB should be connected as close as possible to the respective terminals of the AMT49700.

GROUNDING

A star ground system, with the common star point located close to the AMT49700 is recommended. All ground terminals must be connected together externally. The copper ground plane located under the exposed thermal pad is typically used as the star ground point.

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INPUT/OUTPUT STRUCTURES

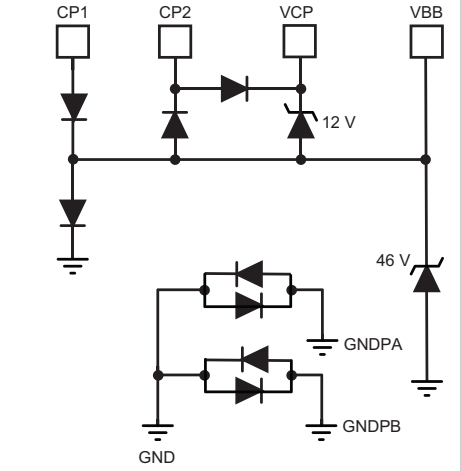

Figure 25a: Supplies and Reference

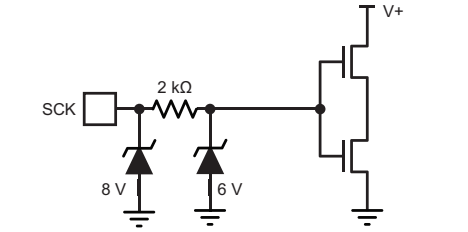

Figure 25b: SCK Input

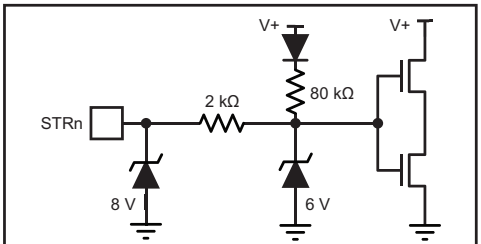

Figure 25c: STRn Input

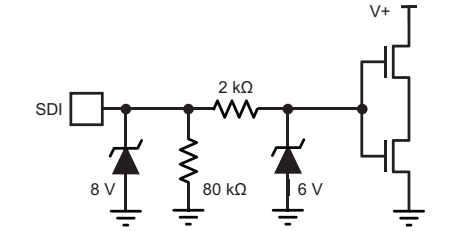

Figure 25d: SDI Input

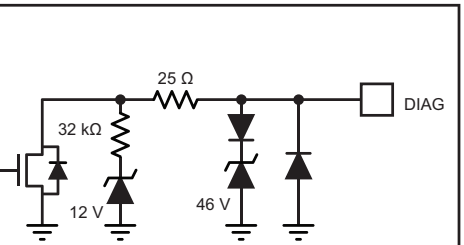

Figure 25g: DIAG Output

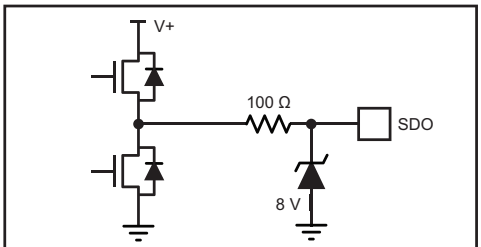

Figure 25e: SDO Output

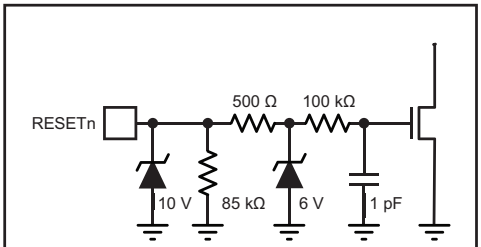

Figure 25h: RESETn, Input

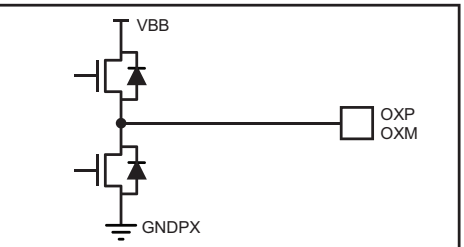

Figure 25i: PHASE Outputs

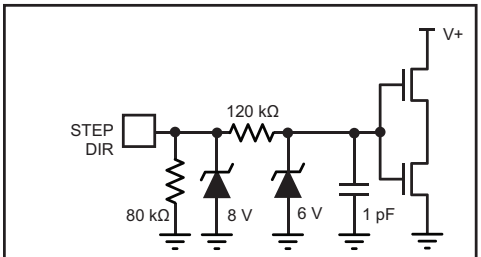

Figure 25j: STEP, DIR Inputs

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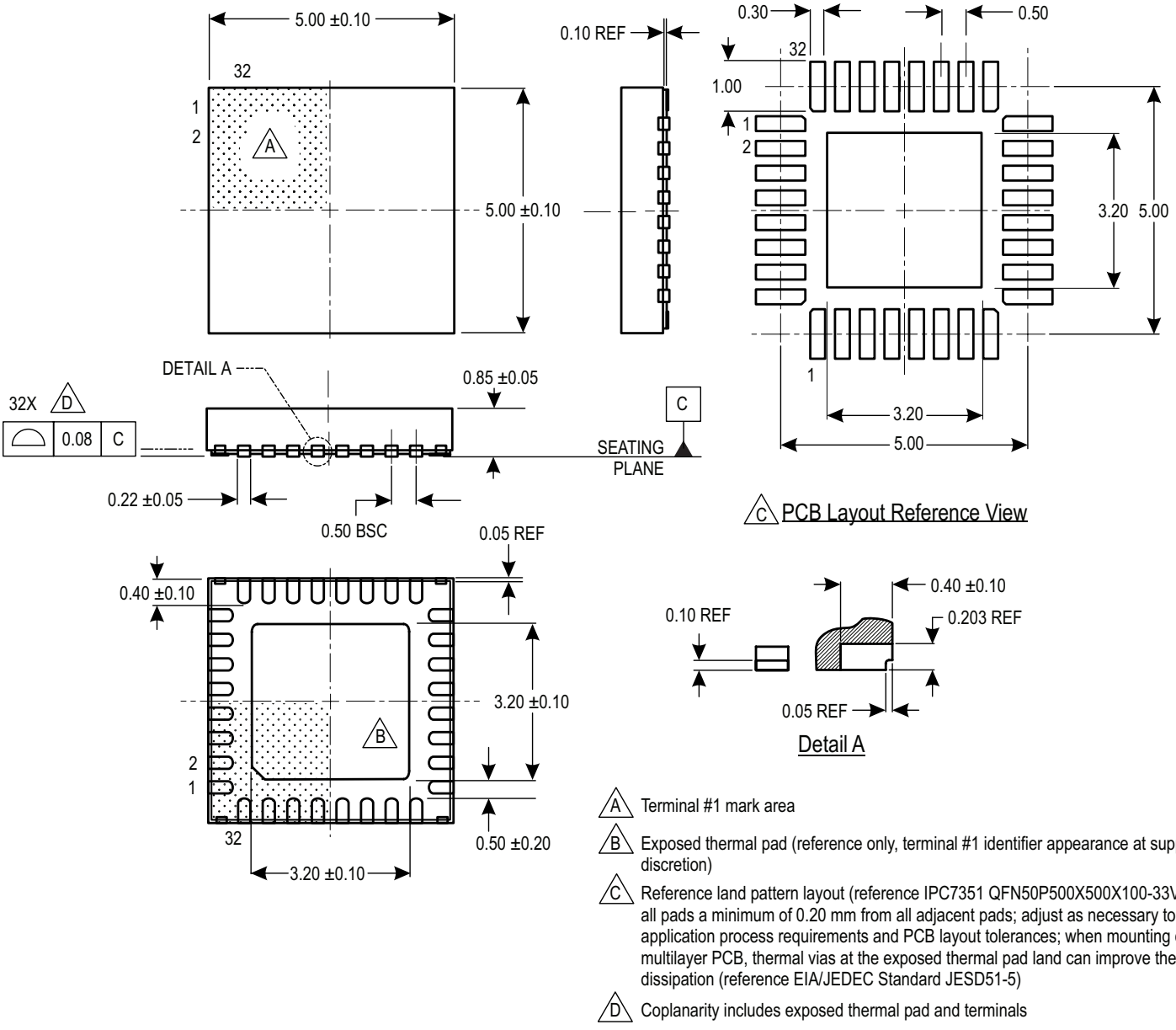
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-220VHHD-6)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-33V6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Figure 26: Package LP, 20-Pin TSSOP with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	February 15, 2019	Initial release
1	June 7, 2019	Updated Phase Current Control section text from “PM[2:0]” to “PM[4:0]” (page 15).

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