2D Dual-Channel Ultrasensitive Hall-Effect Latch

FEATURES AND BENEFITS

- 2D magnetic sensing via planar and vertical Hall elements
  □ Quadrature outputs
  □ 90° phase separation between channels
- Dual-channel output allows independent use of Z-axis planar Hall in conjunction with vertical Hall:
  □ Y-axis (default option)
  □ X-axis (with -X option)
- High sensitivity, B_{OP} typically 17 G
- Automotive grade
  □ AEC-Q100 qualified for use in automotive applications (L temperature range option)
  □ Output short-circuit protection
  □ Resistant to physical stress
  □ Reverse-battery protection
  □ Superior temperature stability
  □ Supply voltage Zener clamp
- Small size

TYPICAL APPLICATIONS

- Automotive
  □ Blower fans
  □ Electric pumps
  □ Electronic power steering
  □ Seat motors
  □ Trunk/liftgate motors
  □ Window/sunroof motors
- Industrial, Commercial, and Consumer
  □ Garage doors
  □ Industrial motors
  □ Motorized window blinds
  □ Motorized gates
 □ Pumps
  □ White goods

DESCRIPTION

The A1262 is a two channel, latching Hall-effect sensor IC that features both vertical and planar Hall elements. The vertical and planar Hall elements feature sensing axes that are orthogonal to one another and provide 90° of phase separation for ring magnets that is inherently independent of magnet pole spacing and air gap.

The 2D architecture of the A1262 simplifies the design of motors and magnetic encoders by providing quadrature output signals in a very small footprint. The A1262 outputs allow the speed and direction of a rotating ring magnet to be determined.

The A1262 is available in two sensing options that allow flexibility in end-system magnetic design. Both options feature a planar Hall plate that is sensitive to magnetic fields perpendicular to the face of the package (Z). Two options of vertical Hall plate orientation (X or Y) in both packages offer flexibility in system design and magnet to sensor placement.

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PACKAGES:

4-Pin SIP (Suffix K)

5-Pin SOT23W (Suffix LH)

Not to scale
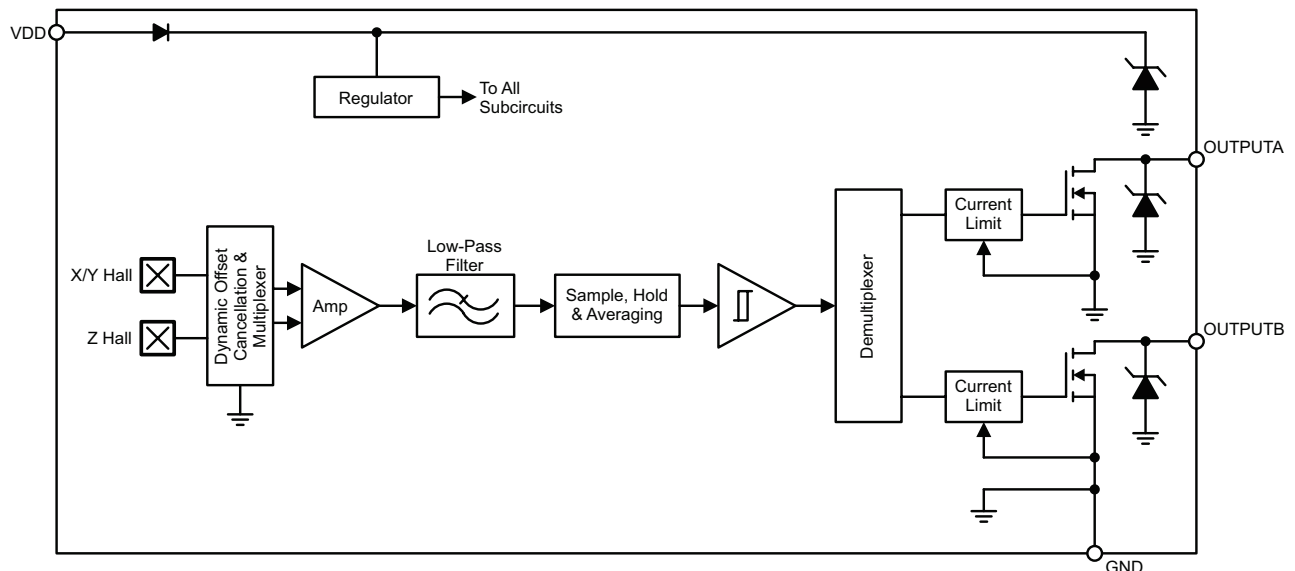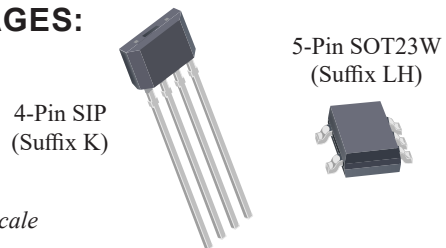
Functional Block Diagram

A1262 — 2D Dual-Channel Ultrasensitive Hall-Effect Latch

DESCRIPTION (continued)

On a single silicon chip, the A1262 includes: voltage regulator, reverse battery protection, two Hall plates (one planar and one vertical), a multiplexer, a small-signal amplifier, chopper stabilization, a Schmitt trigger, and two short-circuit protected open-drain outputs that can sink up to 20 mA continuously.

The A1262 is available in two temperature ranges: –40°C to 85°C (E temperature range option) or –40°C to 150°C (L temperature range option).

The A1262 is available in a 5-pin SOT23W surface-mount package (LH) and a 4 pin SIP package (K). Each is offered in two options for a variety of magnet to sensor orientations. The packages are RoHS compliant and lead (Pb) free, with 100% matte-tin leadframe plating.

SELECTION GUIDE

| Part Number	Packing	Package	Temperature Range, T_A (°C)	Description
A1262ELHLT-T	7-in. reel, 3000 pieces/reel	5-pin SOT-23W surface mount	–40 to 85	2 Outputs of Y and Z
A1262ELHLX-T	13-in. reel, 10000 pieces/reel	5-pin SOT-23W surface mount		
A1262LK-Y-T	Bulk bag, 500 pieces/bag	4-pin SIP through-hole	–40 to 150	
A1262LLHLT-T	7-in. reel, 3000 pieces/reel	5-pin SOT-23W surface mount		
A1262LLHLX-T	13-in. reel, 10000 pieces/reel	5-pin SOT-23W surface mount		
A1262ELHLT-X-T	7-in. reel, 3000 pieces/reel	5-pin SOT-23W surface mount	–40 to 85	2 Outputs of X and Z
A1262ELHLX-X-T	13-in. reel, 10000 pieces/reel	5-pin SOT-23W surface mount		
A1262LK-X-T	Bulk bag, 500 pieces/bag	4-pin SIP through-hole	–40 to 150	
A1262LLHLT-X-T	7-in. reel, 3000 pieces/reel	5-pin SOT-23W surface mount		
A1262LLHLX-X-T	13-in. reel, 10000 pieces/reel	5-pin SOT-23W surface mount		
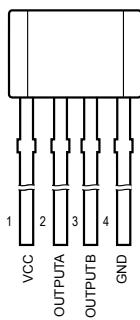
Package K, 4-Pin SIP Pinout
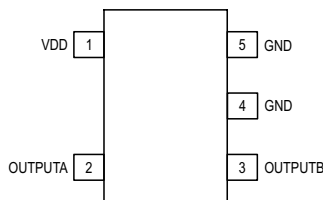
Package LH, 5-Pin SOT23W Pinout

Terminal List Table

Number		Symbol	Description
K	LH		
1	1	VDD	Connects power supply to chip
2	2	OUTPUTA	Output of Z magnetic field direction [1]
3	3	OUTPUTB	Default option: Output of Y magnetic field direction
			With -X option: Output of X magnetic field direction
4	4	GND	Ground
–	5	GND	Ground

[1] Z-axis recommended for use as the speed channel in a speed and direction application, due to better repeatability.
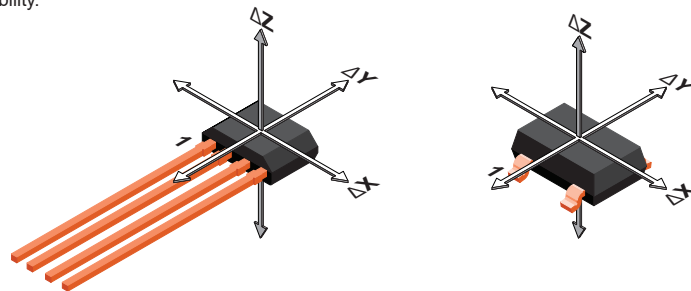
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{DD}		26.5	V
Reverse Supply Voltage	V_{RDD}		−16	V
Magnetic Flux Density	B		Unlimited	G
Output Off Voltage	V_{OUT}		26.5	V
Output Sink Current	$I_{OUT(SINK)}$		Internally Limited	mA
Maximum Junction Temperature	$T_{J(MAX)}$		165	°C
		For 500 hours	175	°C
Storage Temperature	T_{stg}		−65 to 170	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Notes	Rating	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package K, single-sided PCB with copper limited to solder pads	177	°C/W
		Package LH-5 4-layer board based on the JEDEC standard	124	°C/W

* Additional thermal information available on the Allegro website.
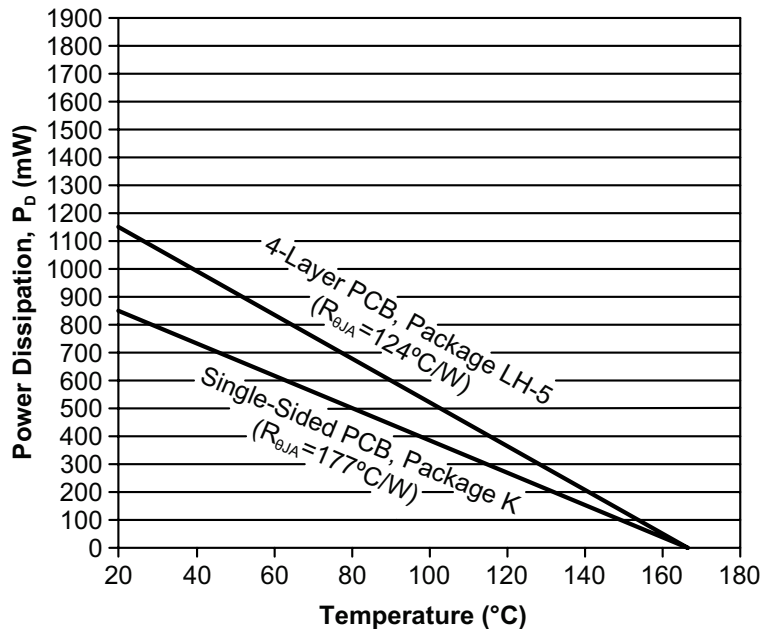
Maximum Power Dissipation versus Ambient Temperature

ELECTRICAL CHARACTERISTICS: Valid over full operating voltage and T_A = –40°C to 85°C (Range E) or T_A = –40°C to 150°C (Range L), unless otherwise specified.

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
Forward Supply Voltage	V_{DD}	Operating, T_J < 165°C	4	–	24	V
Output Leakage Current	I_{OUTOFF}	B < B_{RP}	–	–	10	µA
Output On Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	–	180	500	mV
Supply Current	I_{DD}		2	3	4.5	mA
Reverse-Battery Current	I_{RDD}	V_{RDD} = –16 V	–	–	–5	mA
Supply Zener Clamp Voltage	V_Z	I_{CC} = 5 mA; T_A = 25°C	28	34	–	V
Output Current	I_{OUT}		–	–	20	mA
Output Short-Circuit Current Limit	$I_{OUT(SINK)LIM}$	T_J < $T_{J(max)}$, V_{OUT} = 12 V	30	–	60	mA
Output Sink Current, Peak	$I_{OUT(SINK)PK}$	t < 3 seconds	–	–	110	mA
Chopping Frequency	f_C		–	800	–	kHz
Output Rise Time [2][3]	t_r	R_L = 820 Ω, C_S = 20 pF	–	0.2	–	µs
Output Fall Time [2][3]	t_f	R_L = 820 Ω, C_S = 20 pF	–	0.1	–	µs
Power-On Time [2]	t_{ON}	Both channels, V_{DD} > $V_{DD(MIN)}$	–	32	48	µs
Power-On State	POS	V_{DD} > $V_{DD(MIN)}$, t< t_{ON}	Low			–

[1] Typical data are at T_A = 25°C and V_{DD} = 4 V.
[2] Power-on time, rise time, and fall time are guaranteed through device characterization.
[3] C_S = oscilloscope probe capacitance.

MAGNETIC CHARACTERISTICS: Valid over full operating voltage and T_A = –40°C to 85°C (Range E) or T_A = –40°C to 150°C (Range L), unless otherwise specified.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [4]
Operate Point [5]	B_{OP}		1	17	40	G
Release Point [5]	B_{RP}		–40	–17	–1	G
Hysteresis	B_{HYS}	$B_{OP} - B_{RP}$	15	34	68	G
Symmetry: Channel A, Channel B, $B_{OP(A)} + B_{RP(A)}$, $B_{OP(B)} + B_{RP(B)}$	$B_{SYM(A)}$, $B_{SYM(B)}$		–35	–	35	G
Operate Symmetry: $B_{OP(A)} - B_{OP(B)}$	$B_{SYM(AB,OP)}$		–25	–	25	G
Release Symmetry: $B_{RP(A)} - B_{RP(B)}$	$B_{SYM(AB,RP)}$		–25	–	25	G

[4] 1 G (gauss) = 0.1 mT (millitesla)
[5] Applicable to all directions (X/Y and Z).
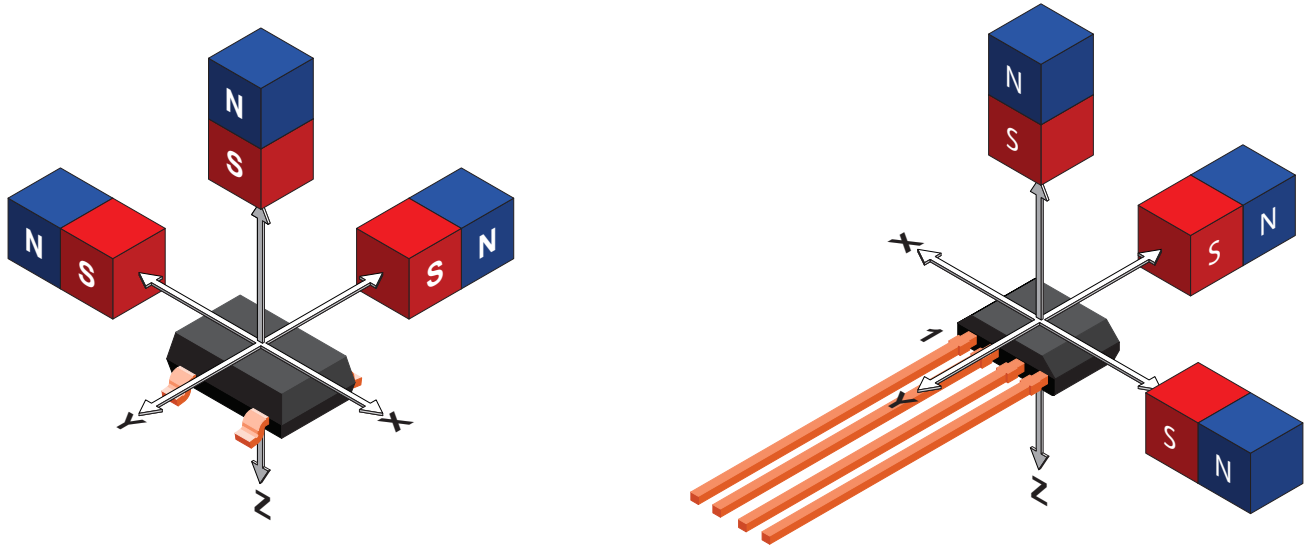
The A1262 output is turned on when presented with a south polarity magnetic field beyond B_{OP} in the orientations illustrated above. The X-axis field response is only applicable to the -X option; the Y-axis field response is only applicable to the default option. Note that magnetic polarity between the LH and K X-axis options are opposite.
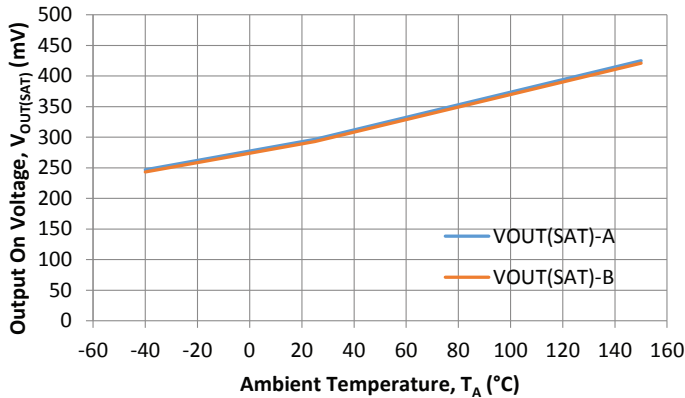
CHARACTERISTIC DATA

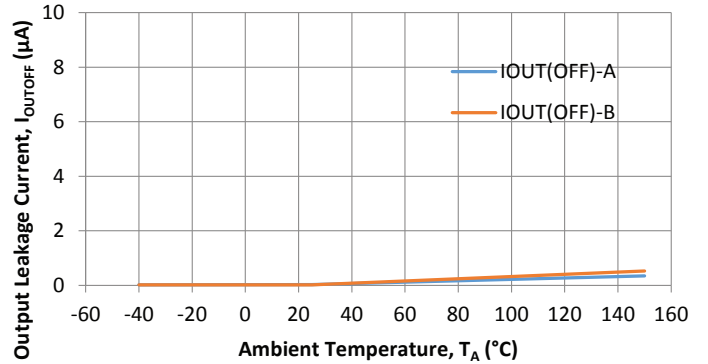### Average Supply Current vs. Ambient Temperature
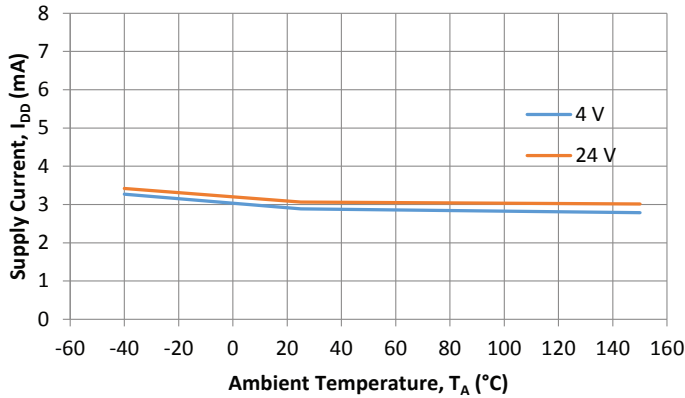
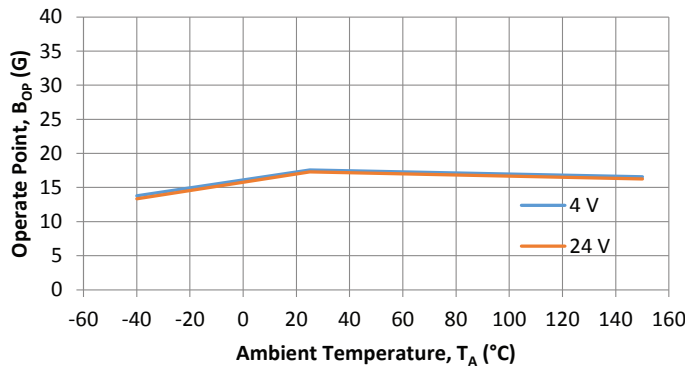### Average Supply Current vs. Supply Voltage
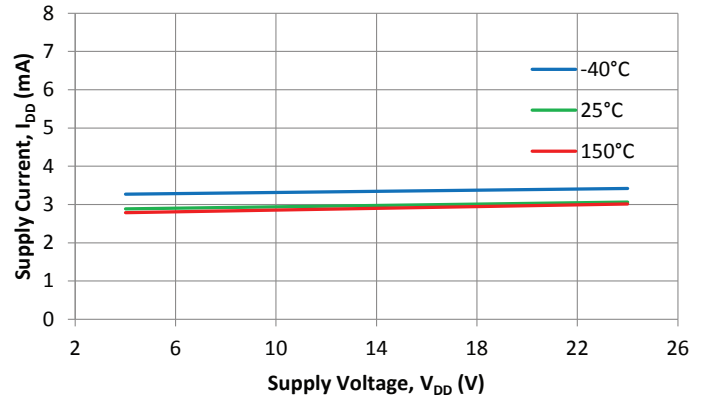
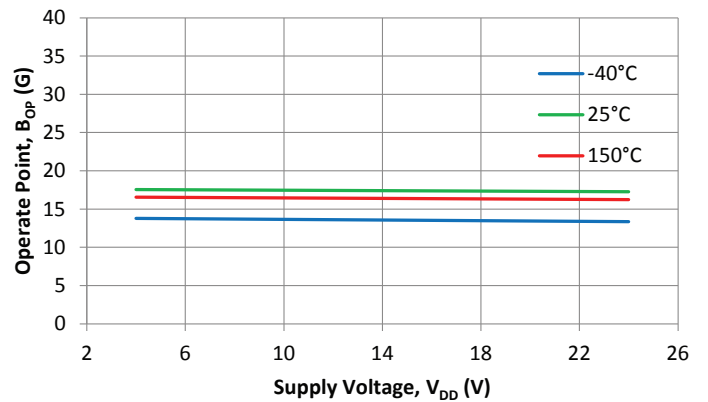### Avg. Output On Voltage vs. Ambient Temperature

Avg. Output Leakage Current vs. Ambient Temperature

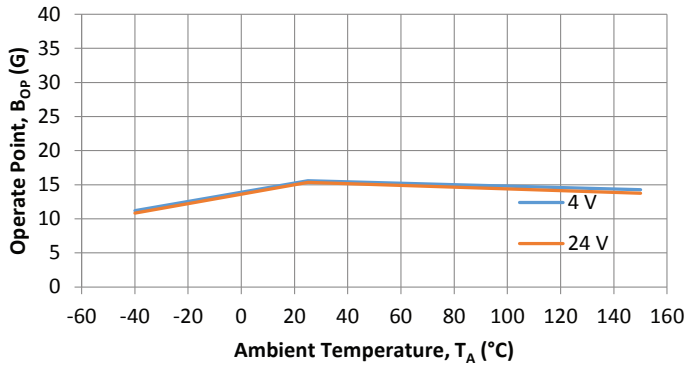
Avg. OUTPUTA Operate Point vs. Ambient Temperature

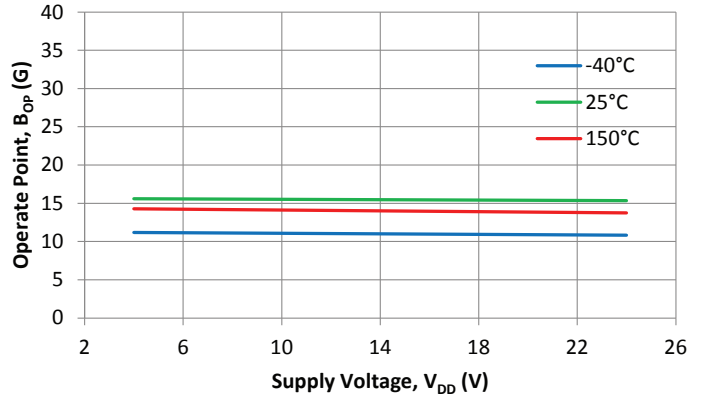### Avg. OUTPUTA Operate Point vs. Supply Voltage

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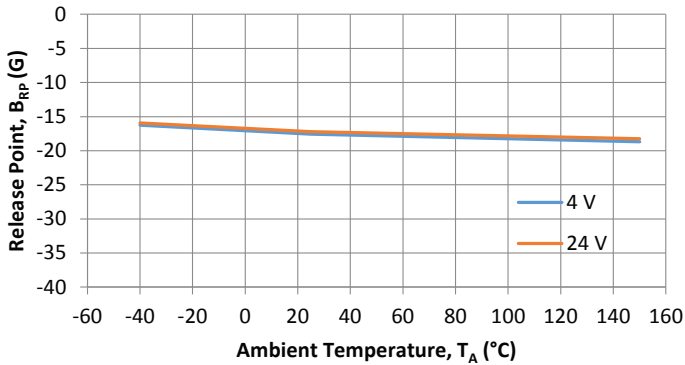## CHARACTERISTIC DATA (continued)

Avg. OUTPUTB Operate Point vs. Ambient Temperature
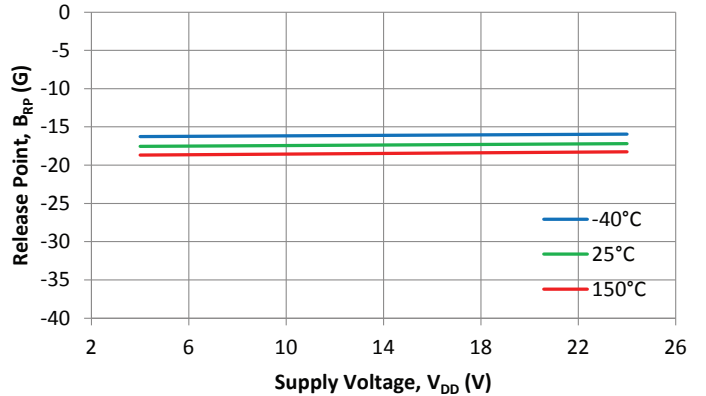
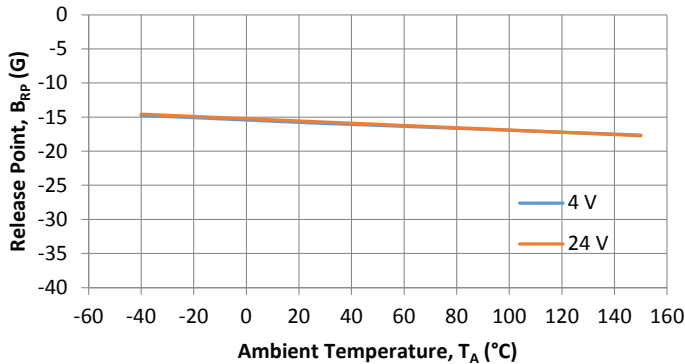**Avg. OUTPUTB Operate Point vs. Supply Voltage**

Avg. OUTPUTA Release Point vs. Ambient Temperature
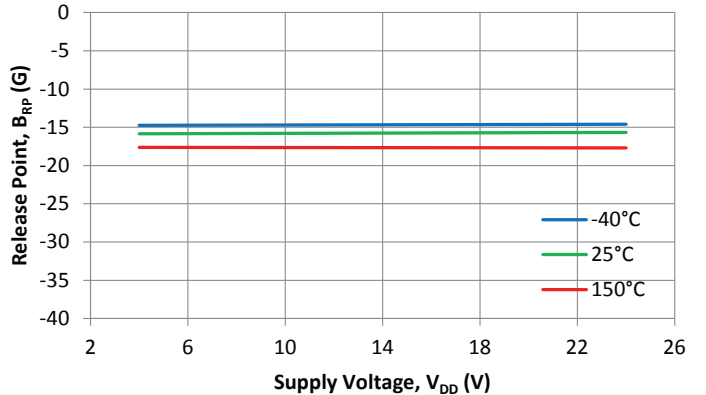
Avg. OUTPUTA Release Point vs. Supply Voltage

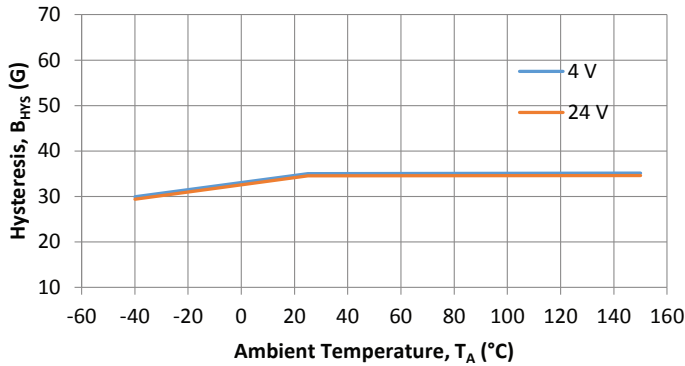**Avg. OUTPUTB Release Point vs. Ambient Temperature**

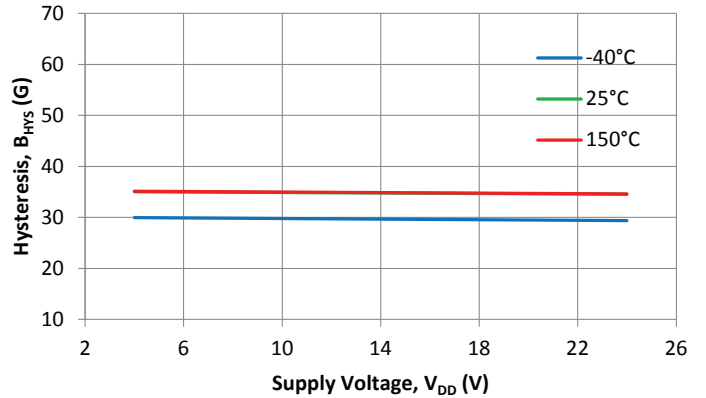**Avg. OUTPUTB Release Point vs. Supply Voltage**

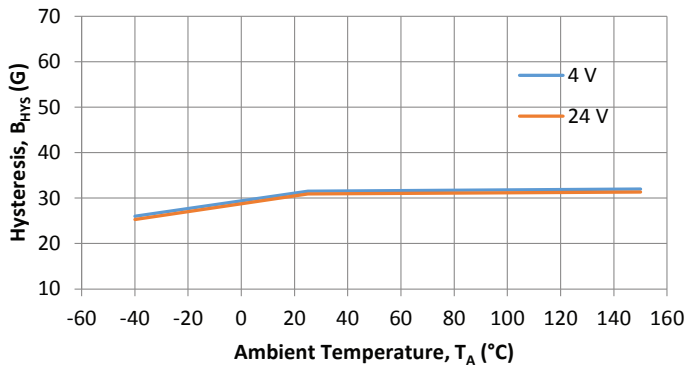## CHARACTERISTIC DATA (continued)

Avg. OUTPUTA Hysteresis vs. Ambient Temperature

Avg. OUTPUTA Hysteresis vs. Supply Voltage

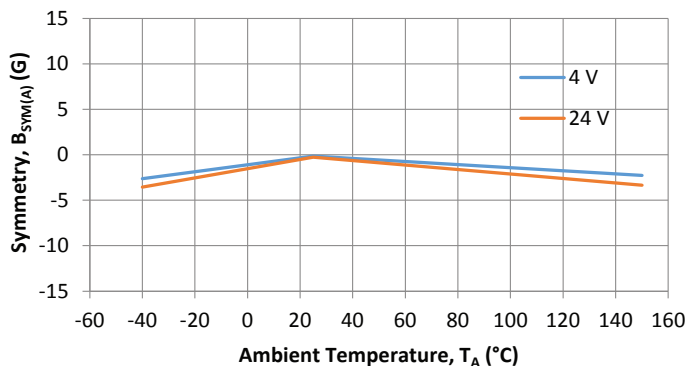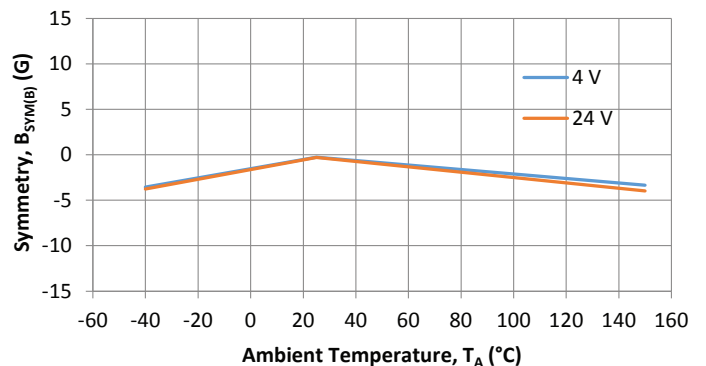**Avg. OUTPUTB Hysteresis vs. Ambient Temperature**

Avg. OUTPUTB Hysteresis vs. Supply Voltage
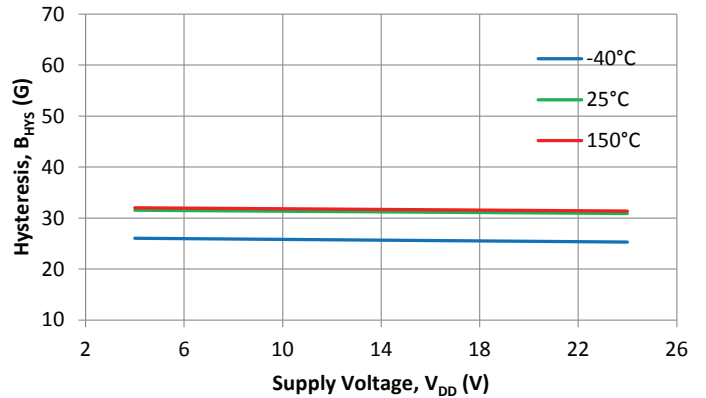
Avg. $B_{OP(A)}+B_{RP(A)}$ Symmetry vs. Ambient Temperature
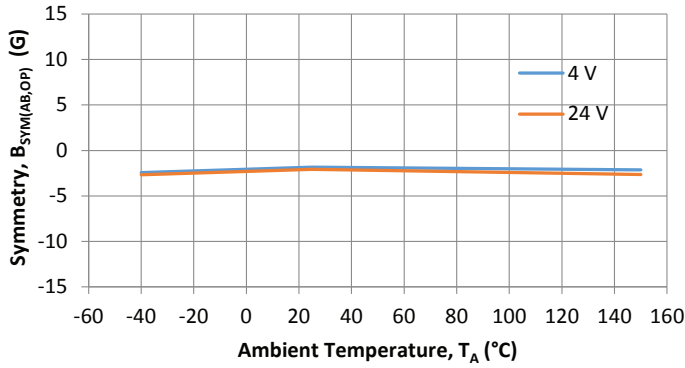

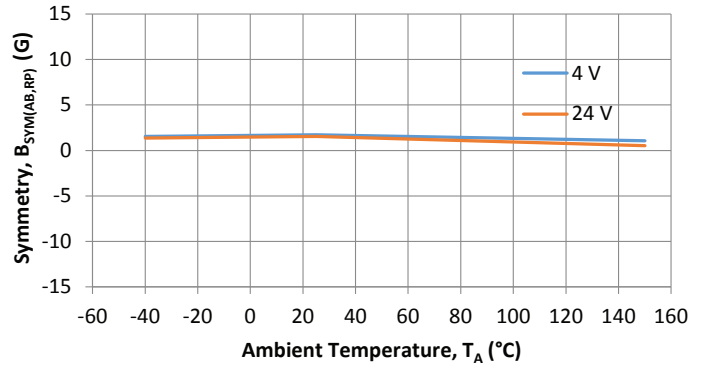**Avg. $B_{OP(B)}+B_{RP(B)}$ Symmetry vs. Ambient Temperature**

CHARACTERISTIC DATA (continued)

Avg. B$_{OP(A)}$–B$_{OP(B)}$ Symmetry vs. Ambient Temperature

Avg. B$_{RP(A)}$–B$_{RP(B)}$ Symmetry vs. Ambient Temperature

FUNCTIONAL DESCRIPTION

Operation

The outputs of the A1262 switch low (turn on) when the corresponding Hall element is presented with a perpendicular south magnetic field of sufficient strength. OUTPUTA switches low if the Z-axis direction exceeds the operate point (B_{OP}), and OUTPUTB switches low if the Y-axis direction (A1262 with default option) or X-axis direction (A1262 with -X option) exceeds B_{OP}. After turn-on, the output voltage is $V_{OUT(SAT)}$. The device outputs switch high (turn off) when the strength of a perpendicular north magnetic field exceeds the release point (B_{RP}). The difference in the magnetic operate and release points is the hysteresis (B_{HYS}) of the device. See Figure 1.

Removal of the magnetic field will leave the device output latched on if the last crossed switch point is B_{OP}, or latched off if the last crossed switch point is B_{RP}.

This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise. The device will power-on in the low output state, even when powering-on in the hysteresis region, between B_{OP} and B_{RP}.

Unlike dual-planar Hall-effect sensors, which have two planar Hall-effect sensing elements spaced apart across the width of the package, both the vertical and planar sensing elements on the A1262 are located in essentially the same location on the IC.
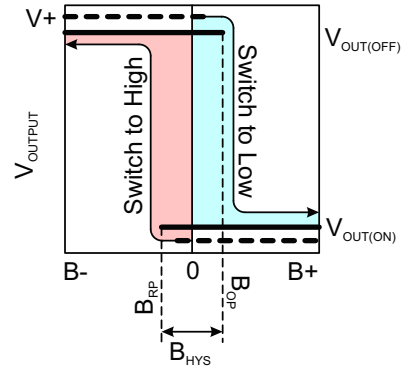

Figure 1: Switching Behavior of Latches

On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity

With dual-planar Hall sensors, the ring magnet must be properly designed and optimized for the physical Hall spacing (distance) in order to have the outputs of the two latches to be in quadrature, or 90 degrees out of phase. With the A1262, which uses one planar and one vertical Hall-effect sensing element, no target optimization is required. When the face of the IC is facing the ring magnet, the planar Hall senses the magnet poles and the vertical Hall senses the transition between poles, therefore the
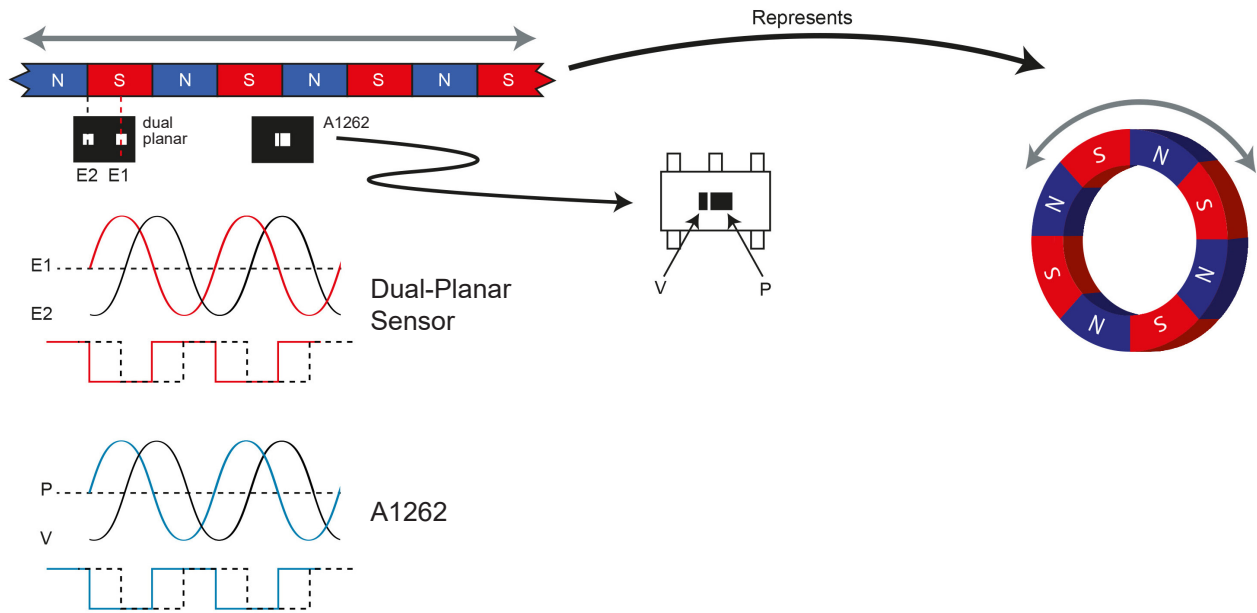

Figure 2: Ring magnet optimized for a dual-planar Hall-effect sensor resulting in output quadrature also results in quadrature for the A1262.

two channels will inherently be in quadrature, irrespective of the ring-magnet pole spacing.

Figure 2 above shows a ring magnet optimized for the E1-to-E2 spacing of a dual-planar sensor, resulting in quadrature, or 90 degrees phase separation between channels. This same target also results in quadrature for the 2D sensing A1262. However when a different ring magnet is used which is not optimized for

the E1-to-E2 spacing, the dual-planar sensor exhibits diminished phase separation, making signal processing the outputs into speed and direction less robust. Using a different ring-magnet geometry has no effect on the A1262, and the two channels remain in quadrature (see Figure 3 below).

The relationship of the various signals and the typical system timing is shown in Figure 4.
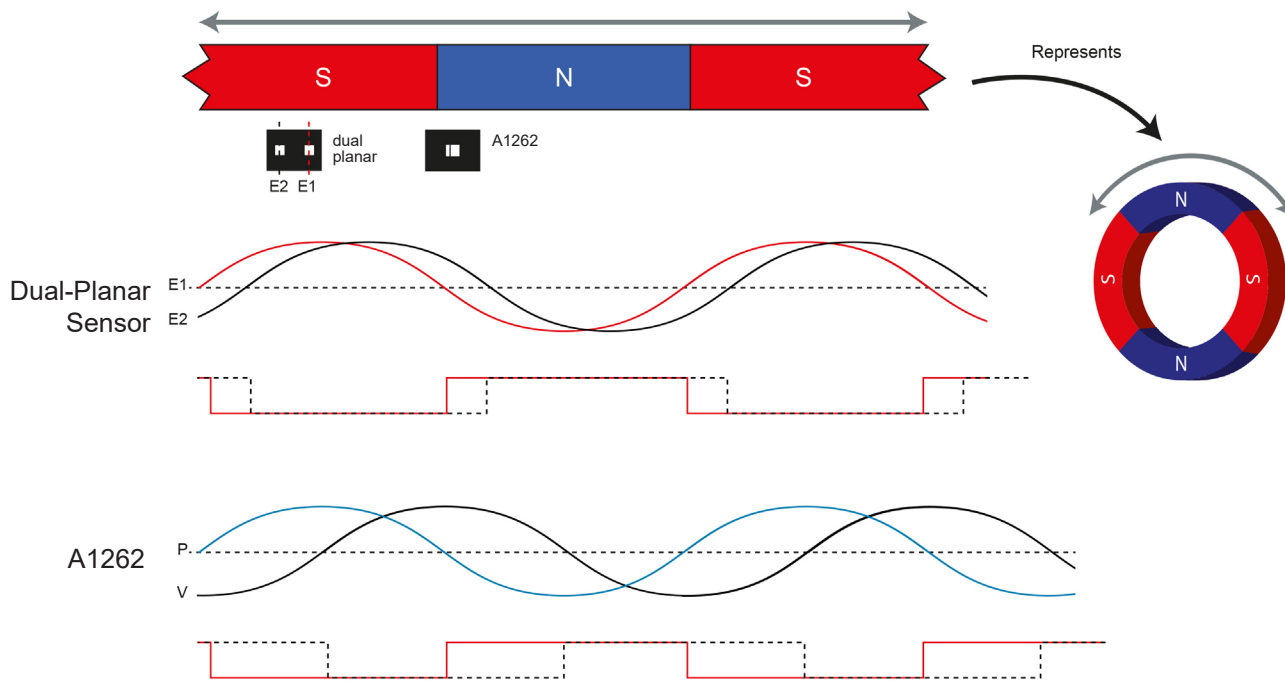
Figure 3: Ring magnet not optimized for a dual-planar Hall-effect sensor resulting in significantly reduced output phase separation, however still results in quadrature for the A1262.

Figure 4: Typical System Timing
The Planar (P) and Vertical (V) signals represent the magnetic input signal, which is converted to the device outputs, OUTPUTA and OUTPUTB, respectively. While the A1262 does not process the signals into Speed and Direction, these could be determined by the user based on the individual output signals.

Figure 5: Typical System Timing

The two active Hall signals represent the magnetic input signal, which is converted to the device outputs, OUTPUTA and OUTPUTB.
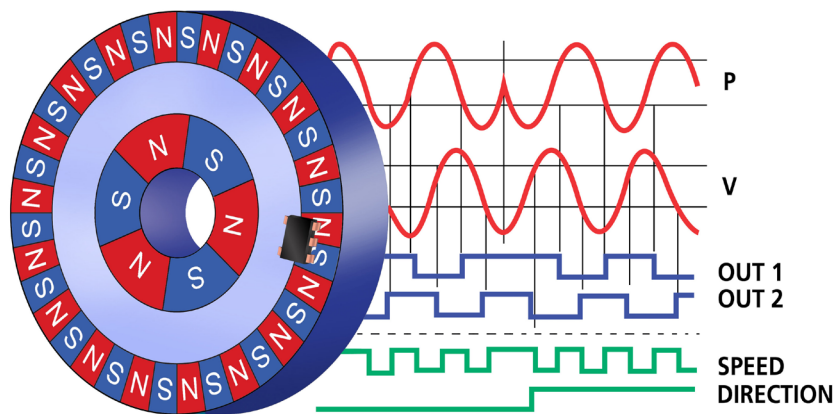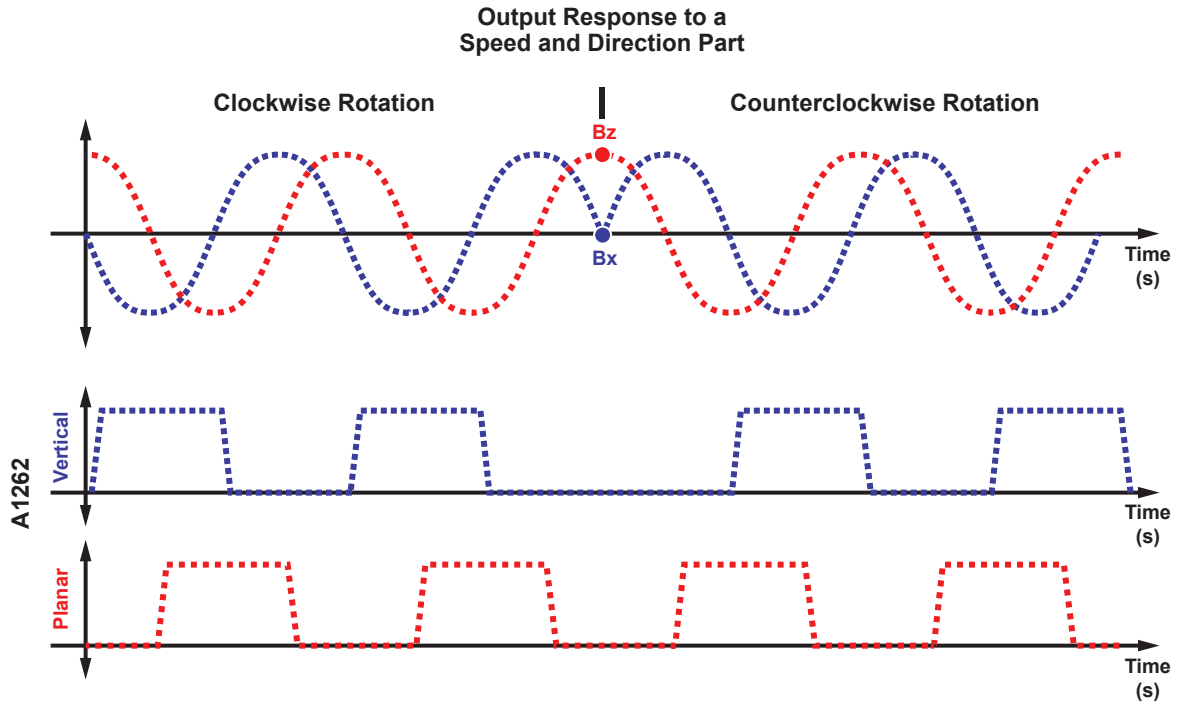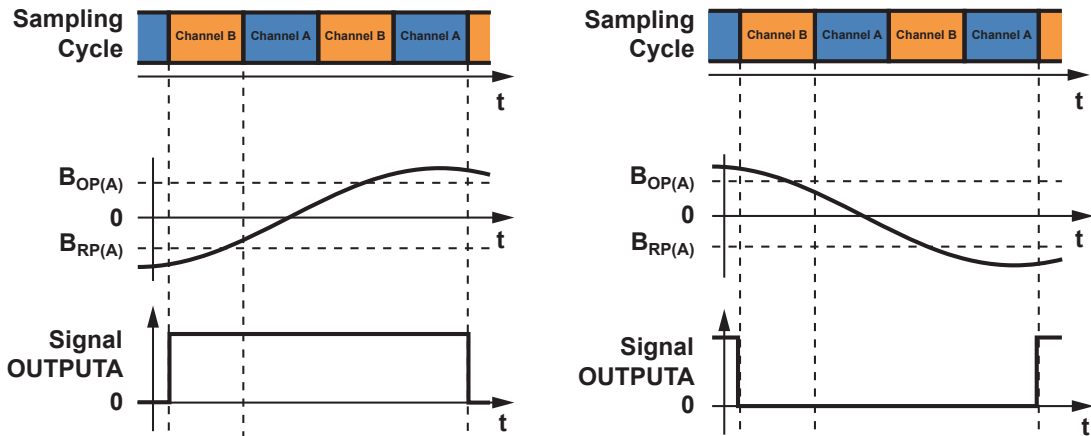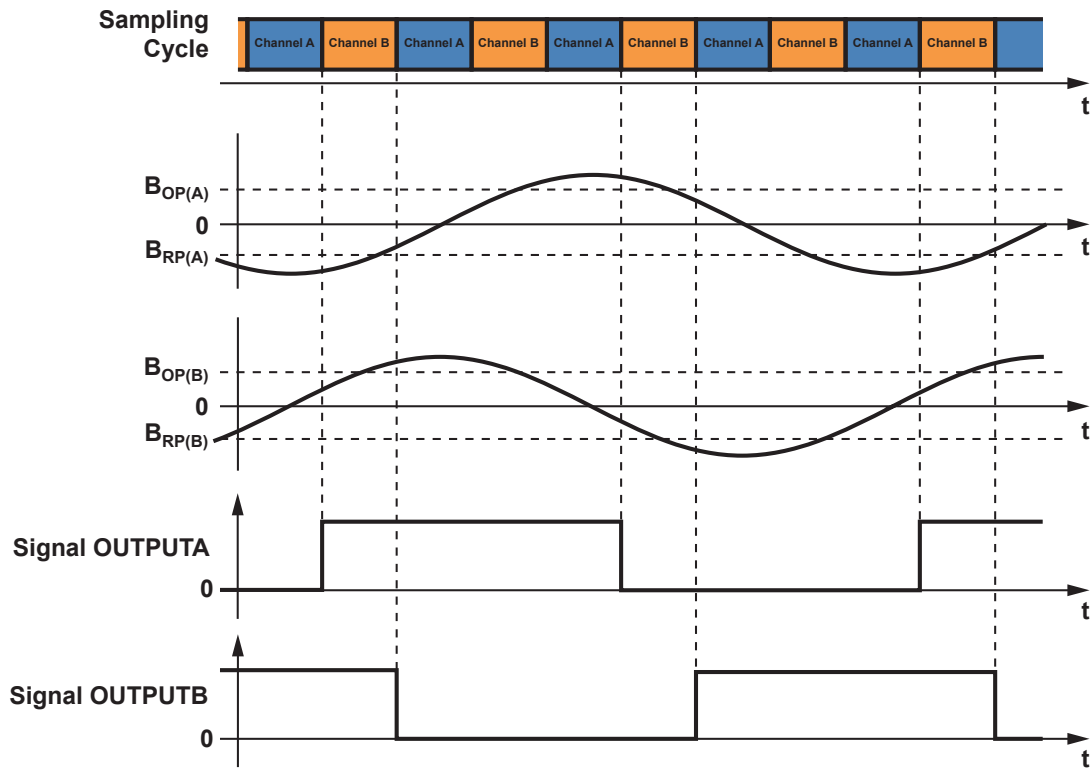
Figure 6: Output signal updating with respect to the channel sampling

The two active channels are multiplexed with a typical 16 μs sampling period per channel. If the magnetic signal crosses the respective B_{OP} or B_{RP} of a particular channel, that channel's output will not be updated until the end of its sampling period. If the signal crosses the thresholds while the alternate channel is sampling, the update will occur at the end of the next sampling period (as long as the signal does not cross back over the thresholds). This is illustrated in Figure 6. The sampling error introduced by the multiplexing increases with magnetic input frequency, which can affect the output duty cycle and phase separation between outputs. Contact your Allegro representative for more information regarding suitability to high frequency applications.

A1262 Sensor and Relationship to Target

The A1262 is available in two sensing options: with Z-axis planar Hall and the Y-axis vertical Hall active (default option), or with the Z-axis planar Hall and the X-axis vertical Hall active (-X option). This offers incredible flexibility for positioning the IC within various applications.

The Z-Y option supports the traditional configuration with the face of the package facing the ring magnet (Figure 7a or 7c), with the axis of rotation going cross the leads, or opposide the leaded side(s) of the package facing the ring magnet (Figure 7b or 7d).
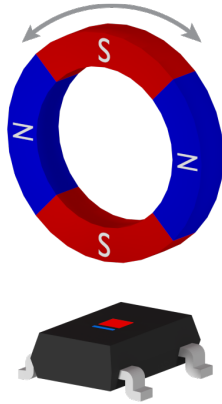
Figure 7a: LH (-Y option)
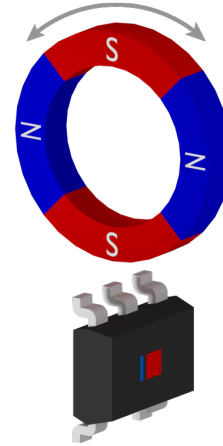
Figure 7b: LH (-Y option)
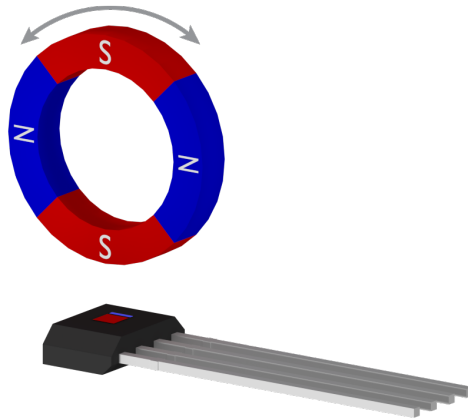
Figure 7c: K (-Y option)
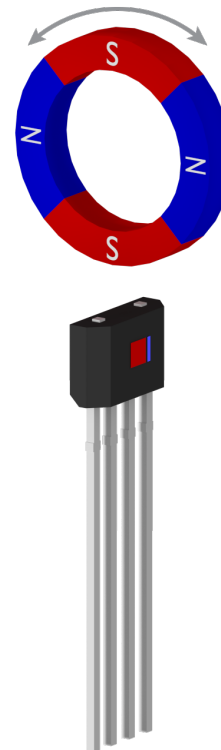
Figure 7d: K (-Y option)

The Z-X option supports having the IC positioned with the face of the package facing the ring magnet, and the axis of rotation (Figure 8a or 8c) lengthwise along the package body, or with either of the non-leaded sides of the package facing the ring mag-net (Figure 8b or 8d). This latter configuration has the advantage of being able to be mounted extremely close to the ring magnet, since there are no leads or solder pads to accommodate for in that dimension.
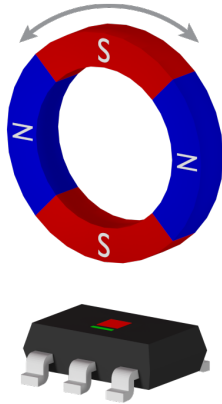
Figure 8a: LH (-X option)
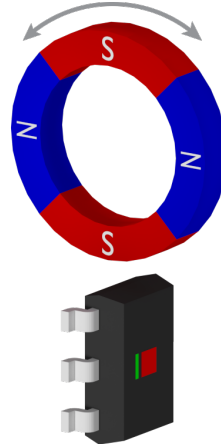
Figure 8b: LH (-X option)
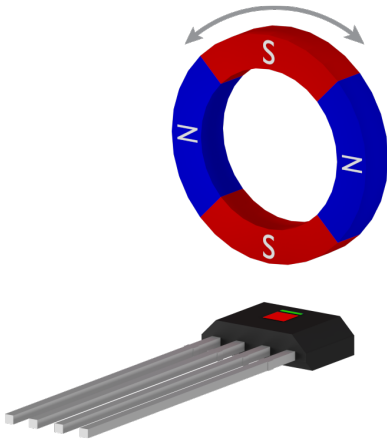
Figure 8c: K (-X option)
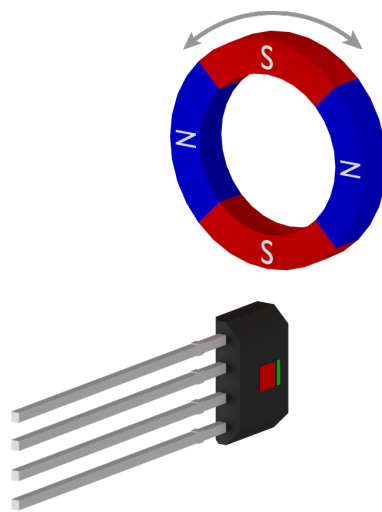
Figure 8d: K (-X option)

Power-On Sequence and Timing

The states of OUTPUTA and OUTPUT B are only valid when the supply voltage is within the specified operating range ($V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$) and the power-on time has elapsed ($t > t_{ON}$). Refer to Figure 9: Power-On Sequence and Timing for an illustration of the power-on sequence.
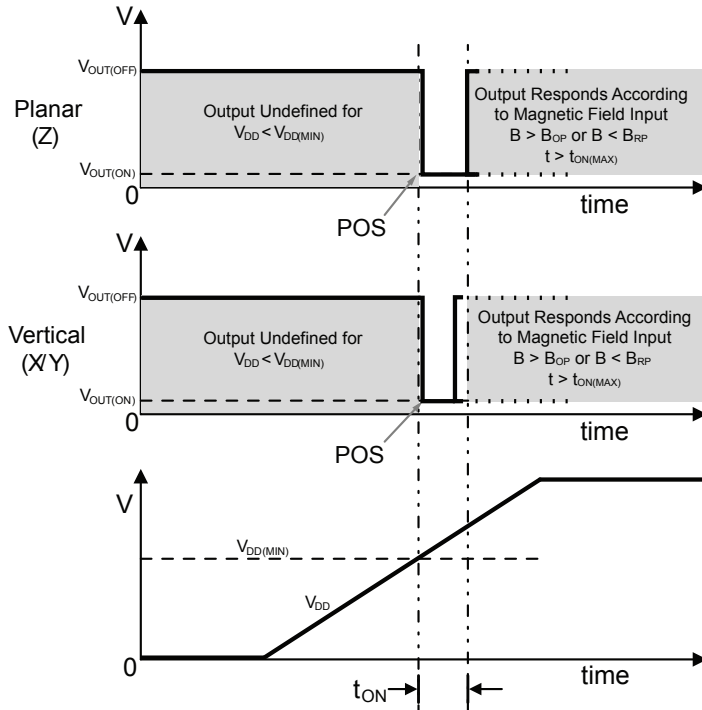
Figure 9: Power-On Sequence and Timing

Once the supply voltage is within the operational range, the outputs will be in the low state (power-on state), irrespective of the magnetic field. The outputs will remain low until the sensor is fully powered on ($t > t_{ON}$), at which point, both outputs will respond to the corresponding magnetic field presented to the sensor (the vertical Hall channel typically responds before the planar Hall channel).

Applications

It is strongly recommended that an external capacitor be connected (in close proximity to the Hall sensor) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization technique. As shown in Figure 10, a 0.1 µF capacitor is typical.
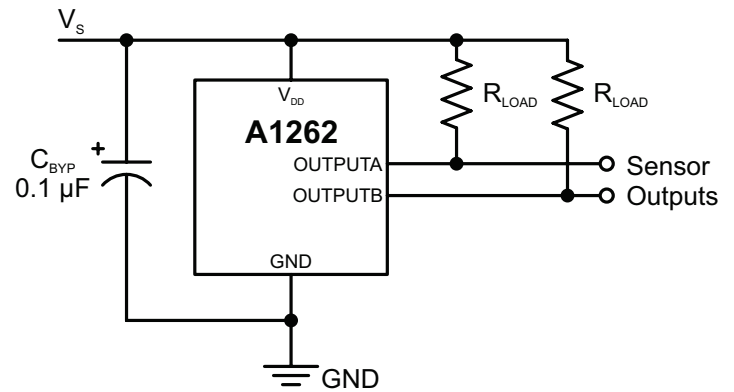
Figure 10: Typical Application Circuit

Extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide, AN27701,*

- *Hall-Effect Devices: Guidelines for Designing Subassemblies Using Hall-Effect Devices, AN27703.1*

- *Soldering Methods for Allegro's Products – SMD and Through-Hole, AN26009*

- *Air-Gap-Independent Speed and Direction Sensing Using the Allegro A1262, AN296124*

- *Improved Speed and Direction Sensing Using Vertical Hall Technology, AN296130*

All are provided on the Allegro website:

www.allegromicro.com

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switch-point accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a proven approach used to minimize Hall offset on the chip. The Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of output drift induced by thermal and mechanical stresses. This technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field induced signal to recover its original spectrum at baseband, while the DC offset becomes a high-frequency signal. The magnetic sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. This configuration is illustrated in Figure 11.

The chopper stabilization technique uses a 400 kHz high-frequency clock. For demodulation process, a sample, hold, and averaging technique is used, where the sampling is performed at twice the chopper frequency (800 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic and sample-and-hold circuits.
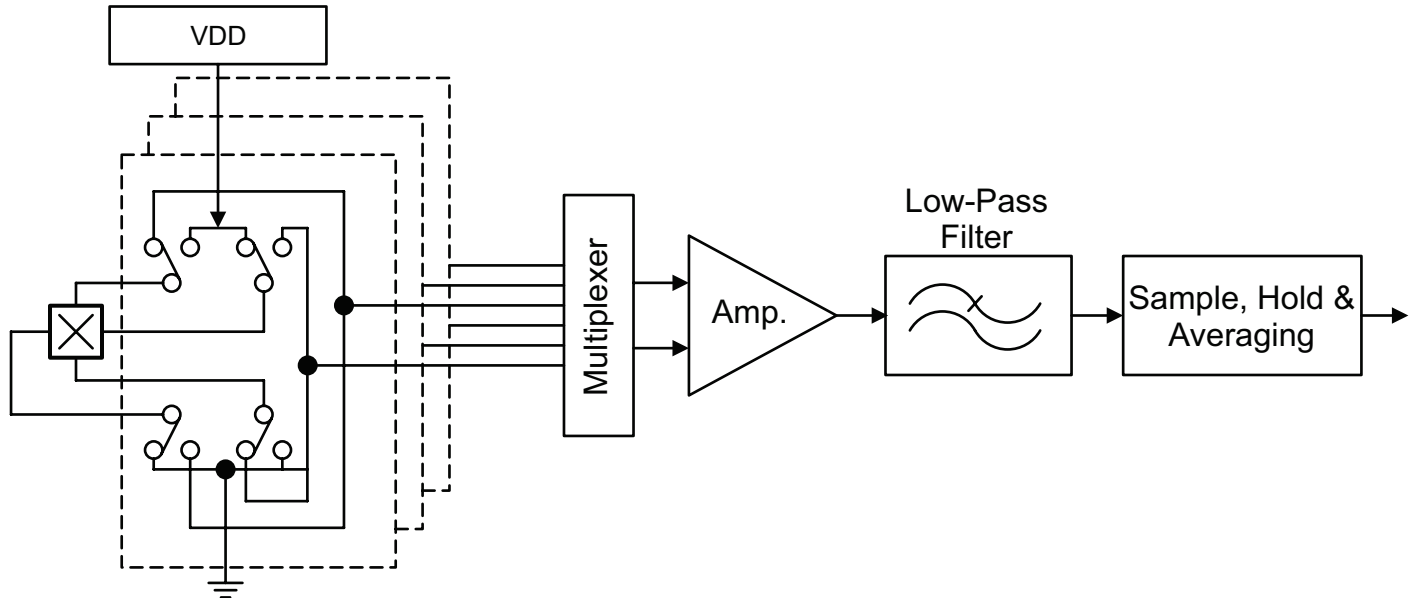

Figure 11: Model of Chopper Stabilization Technique

POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is relatively small component of $R_{\theta JA}$. Ambient air temperature (T_A) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J at P_D.

$$P_D = V_{IN} \times I_{IN} \qquad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \qquad (2)$$

$$T_J = T_A + \Delta T \qquad (3)$$

For example, given common conditions such as: $T_A = 25°C$, $V_{DD} = 12$ V, $I_{DD} = 3$ mA, and $R_{\theta JA} = 124°C/W$ for the LH5 package, then:

$$P_D = V_{DD} \times I_{DD} = 12 \ V \times 3.0 \ mA = 36.0 \ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 36.0 \ mW \times 124°C/W = 4.5°C$$

$$T_J = T_A + \Delta T = 25°C + 4.5°C = 29.5°C$$

A worst-case estimate ($P_{D(max)}$) represents the maximum allowable power level ($V_{DD(max)}$, $I_{DD(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{DD} at $T_A = 150°C$, package LH5, using low-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA} = 124°C/W$, $T_{J(max)} = 165°C$, $V_{DD(max)} = 24$ V, and $I_{DD(max)} = 7.5$ mA.

Calculate the maximum allowable power level ($P_{D(max)}$). First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 124°C/W = 121 \ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{DD(est)} = P_{D(max)} \div I_{DD(max)}$$

$$V_{DD(est)} = 121 \ mW \div 7.5 \ mA$$

$$V_{DD(est)} = 16.1 \ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{DD(est)}$.

Compare $V_{DD(est)}$ to $V_{DD(max)}$. If $V_{DD(est)} \leq V_{DD(max)}$, then reliable operation between $V_{DD(est)}$ and $V_{DD(max)}$ requires enhanced $R_{\theta JA}$. If $V_{DD(est)} \geq V_{DD(max)}$, then operation between $V_{DD(est)}$ and $V_{DD(max)}$ is reliable under these conditions.
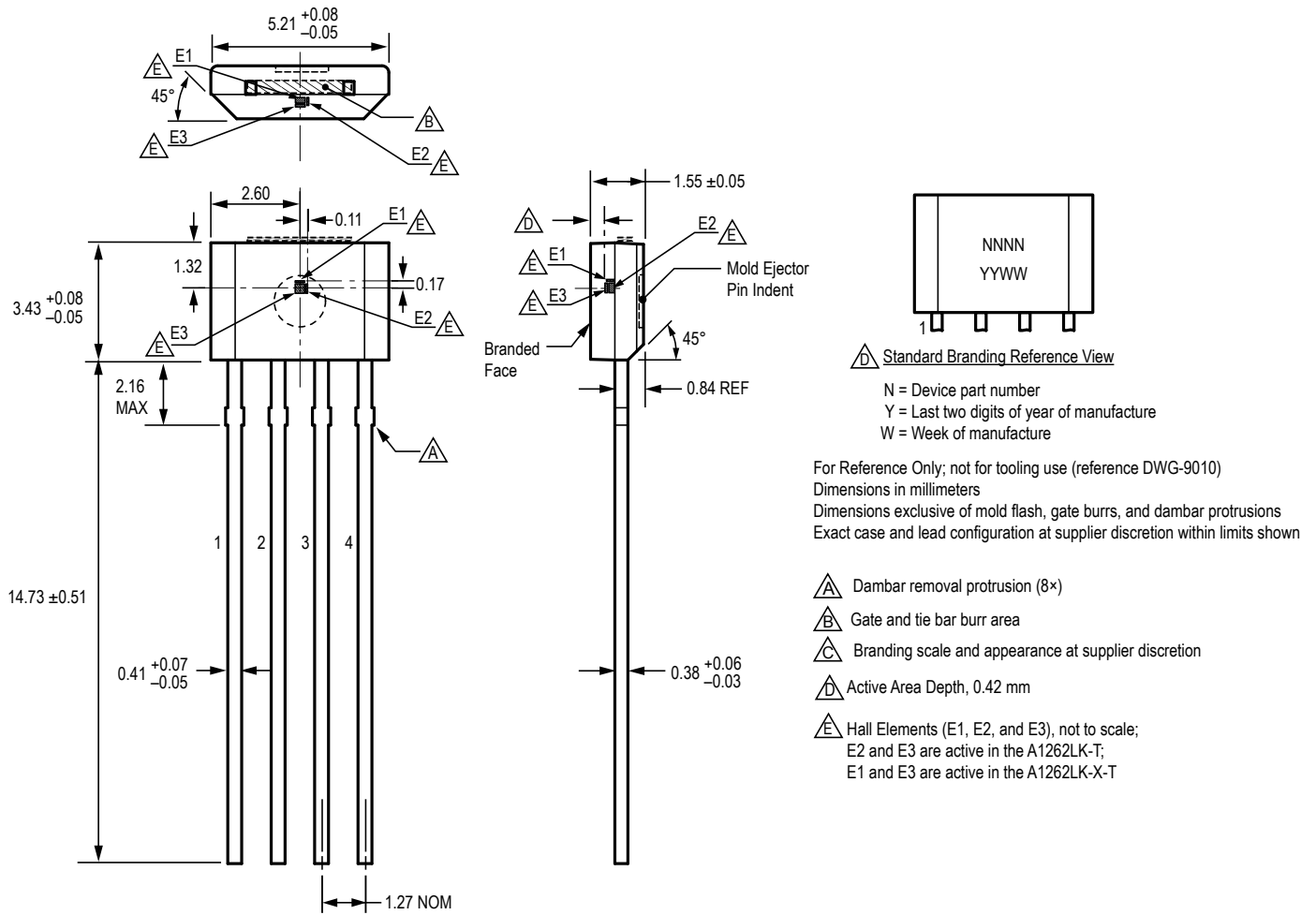
PACKAGE OUTLINE DRAWINGS

5.21 +0.08 −0.05

45°

E1

E3

E2

2.60

0.11

1.32

3.43 +0.08 −0.05

2.16 MAX

E1

E3

E2

14.73 ±0.51

0.41 +0.07 −0.05

1 2 3 4

1.27 NOM

0.17

1.55 ±0.05

E1

E3

E2

Mold Ejector Pin Indent

Branded Face

45°

0.84 REF

0.38 +0.06 −0.03

NNNN

YYWW

1

Standard Branding Reference View

N = Device part number
Y = Last two digits of year of manufacture
W = Week of manufacture

For Reference Only; not for tooling use (reference DWG-9010)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A   Dambar removal protrusion (8×)

B   Gate and tie bar burr area

C   Branding scale and appearance at supplier discretion

D   Active Area Depth, 0.42 mm

E   Hall Elements (E1, E2, and E3), not to scale;
E2 and E3 are active in the A1262LK-T;
E1 and E3 are active in the A1262LK-X-T

Figure 12: Package K, 4-Pin SIP

For Reference Only – Not for Tooling Use
(Reference DWG-9069)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
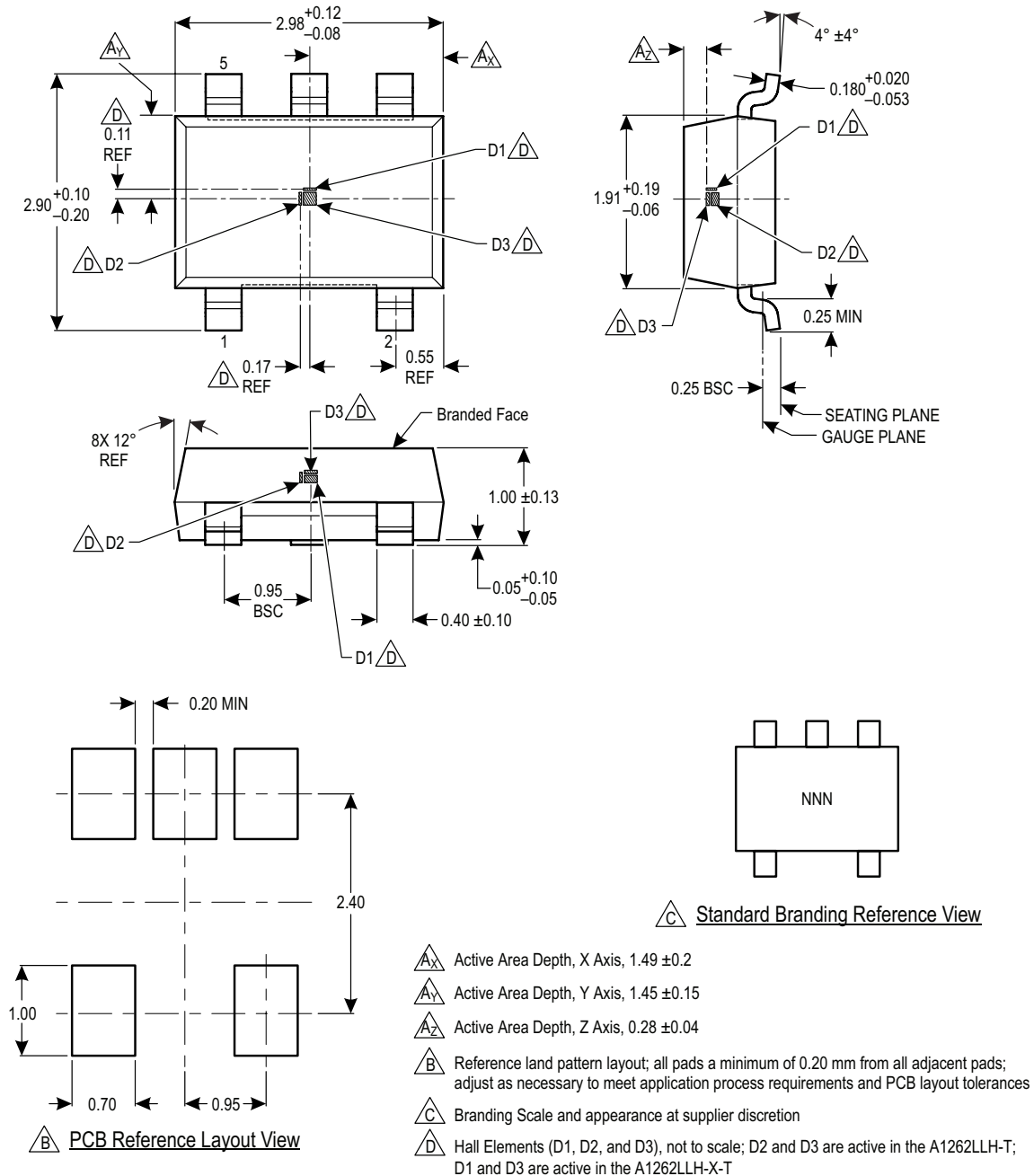Exact case and lead configuration at supplier discretion within limits shown

Standard Branding Reference View

PCB Reference Layout View

A_X Active Area Depth, X Axis, 1.49 ±0.2

A_Y Active Area Depth, Y Axis, 1.45 ±0.15

A_Z Active Area Depth, Z Axis, 0.28 ±0.04

B Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding Scale and appearance at supplier discretion

D Hall Elements (D1, D2, and D3), not to scale; D2 and D3 are active in the A1262LLH-T; D1 and D3 are active in the A1262LLH-X-T

Figure 13: Package LH, 5-Pin SOT23-W

Revision History

Number	Date	Description
–	September 21, 2015	Initial release
1	February 10, 2016	Added E temperature range option and magnetic switch point symmetry specifications
2	February 10, 2017	Updated Features and Benefits (page 1), Description (pages 1-2), Absolute Maximum Ratings table (page 3), Electrical Characteristics table (page 4), Figure 5 (page 12), Figure 6 (page 13), Figure 7 and 8 labels (pages 14-15), Chopper Stabilization section (page 17); added Typical Applications; added K package option; expanded Functional Description section.
3	May 19, 2017	Corrected Pinout Diagrams (page 2).
4	July 31, 2017	Updated Selection Guide table (page 2).
5	August 8, 2018	Minor editorial updates.
6	August 22, 2019	Minor editorial updates.

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