# *AMD E8860*
# *PCIe® ADD-IN BOARD*
# *Datasheet*

## *(GFX-A5T8-20FMT1)*

# CONTENTS

# 1.  Feature

| Model Name | GFX-A5T8-20FMT1 |
|---|---|
| **Graphics Processing Unit** | |
| GPU | AMD Radeon E8860 |
| Process Technology | 28nm |
| GPU TDP | 37W |
| Graphics Engine Operating Frequency (max) | 625Mhz |
| Dimension | ATX Low Profile (160 x 69mm) |
| CPU Interface | PCI Express® 3.0 (x1, x2, x4, x8, x16) |
| Shader Processing Units | 8 SIMD engines x 80 processing elements = 640 shaders |
| Floating Point Performance | 768GFLOPs peak single-precision<br>48FLOPs peak double-precision |
| DirectX® capability | DirectX® 11.1 |
| Shader Model | Shader Model 5.0 |
| OpenGL | OpenGL 4.1+ |
| OpenCL | OpenCL 1.1/1.2+ |
| Unified Video Decoder (UVD) | UVD3 for H.264, VC-1, MPEG-2, MPEG-4 part 2 decode |
| **Memory** | |
| Operating Frequency (max) | 1125 MHZ / 4.5 Gbps |
| Configuration, type | 128-bit wide, 2 GB, GDDR5 |
| **Display Interface** | |
| DisplayPort 1.2 | Mini DisplayPort 1.2 x 4 |

# 2. Functional Overview

## 2.1. Memory Configuration Support

AMD Radeon™ E8860 has four DRAM sequencers. Each DRAM channel is 32-bit wide. Four 128 Mb × 32 GDDR5 memory chips are embedded on the ASIC for a total of 2 GB memory.

## 2.2. Acceleration Features

- Support for all DirectX® 11 features, including the full-speed 32-bit floating point per component operation:
  - Shader Model 5.0 geometry and pixel support in a unified shader architecture:
    - Vertex, pixel, geometry, compute, domain, and hull shaders.
    - 32- and 64-bit floating-point processing per component.
    - New advanced shader instructions, including flexible flow control with CPU-level flexibility on branching.
    - A nearly unlimited shader-instruction store, using an advanced caching system.
    - An advanced shader design, with an ultra-threading sequencer for high-efficiency operations.
    - A new advanced shader core, supporting native scalar instructions.
    - Advanced, high-performance branching support, including static and dynamic branching.
    - High dynamic-range rendering with floating-point blending, texture filtering, and anti-aliasing support.
    - 16- and 32-bit floating-point components for high dynamic-range computations.
    - Full anti-aliasing on renderable surfaces up to and including 128-bit floating-point formats.
    - A new read/write caching system, replacing texture cache with a unified read-write two-level cache.
- Support for OpenGL 4.1/4.1+.
- Support for OpenCL™ 1.1/1.2+.
- Anti-aliasing filtering:
  - 2×/4×/8× MSAA (multi-sample anti-aliasing) modes are supported.
  - A multi-sample algorithm with gamma correction, programmable sample patterns, and centroid sampling.
  - Custom filter anti-aliasing with up to 12-samples per pixel.
  - An adaptive anti-aliasing mode.
  - Lossless color compression (up to 16:1).
- Anisotropic filtering:
  - Continuous anisotropic with 1× through 16× taps.
  - Up to 128-tap texture filtering.
  - Anisotropic biasing to allow trading quality for performance.
  - Improved anisotropic filtering with unified non-power of two-tap distribution and higher precision filter

computations.

- Advanced texture compression (3Dc+™).
- High quality 4:1 compression for normal and luminance maps.
- Angle-invariant algorithm for improved quality.
- Single- or two-channel data format compatibility.

- 3D resources virtualized to a 40-bit virtual addressing space, for support of large numbers of render targets and textures.
- Up to 16k × 16k textures, including 128-bit/pixel texture are supported.
- Programmable arbitration logic maximizes memory efficiency and is software upgradeable.
- Fully associative texture, color, and z-cache design.
- Hierarchical z- and stencil-buffers with early z-test.
- Lossless z-buffer compression for both z and stencil.
- Fast z-buffer clear.
- Fast color-buffer clear.
- Z-cache optimized for real-time shadow rendering.
- Z- and color-compression resources virtualized to a 32-bit addressing space, for support of multiple render targets and textures simultaneously.

## 2.3. Avivo™ Display System

- The AMD Avivo™ display system supports VGA, VESA super VGA, and accelerator mode graphics display on six independent display controllers.
- The full features of the AMD Avivo display system are outlined in the following sections.

- Six independent display controllers that support true 30-bpp (bits per pixel) throughout the display pipe.
- Support for display resolutions up to 4096 × 2160 @ 30 Hz per display output, which do not oversubscribe available memory bandwidth.
- Flexible support for various combinations of display outputs based on clock dependencies:
  - Two internal display PLLs (phase-locked loops) and an integrated DisplayPort reference clock can support:
    - Any two legacy displays and up to four DisplayPorts, or
    - One legacy display and up to five DisplayPorts, or
    - Six DisplayPorts eDP (embedded DisplayPort) is also considered a DisplayPort).
- Advanced video capabilities, including high-fidelity gamma, color correction, and scaling.
- A high-precision color pipe with the support of XR-biased sRGB and xvYCC formats.
- An adaptive per-pixel de-interlacing and frame-rate conversion (temporal filtering).
- An enhanced dithering algorithm for LCD panels.
- Full RMX for sources up to 2560 pixels/line.
- HDCP can be supported on six independent displays, such as HDMI™, DVI, or DisplayPort.
  - **Note:** HDCP is available only to licensed HDCP buyers.
- HDCP Protection:

- ◼ Key information is stored in the ASIC.

- ◼ An external ROM is not needed.

- ◼ Protects both audio and video content on all HDMI/DisplayPort outputs.

- Adaptive backlight modulation to reduce panel-power consumption in embedded applications.

- An improved memory-access pattern to reduce the memory-power consumption in embedded applications.

- 3D display capabilities for both graphic and overlay contents.

## 2.4. DVI/HDMI™/DisplayPort Features

- On TMDSA, TMDSB, TMDSC, and TMDSD the following display configurations are supported.

  - ◼ Two single-link DVIs (any two from TMDSA, TMDSB, TMDSC, and TMDSD)

  - ◼ Two dual-link DVIs

  - ◼ HDMI

- On LVDSE and LVDSF the following display configurations are supported.

- One dual-link LVDS

- One single-link LVDS

- One dual-link DVI

- Two single-link DVIs

- HDMI

  - ◼ On TMDPA, TMDPB, TMDPC, and TMDPD the following display configurations are supported.

- Four version 1.2 DisplayPorts

  - ◼ On LVDPE and LVDPF the following display configurations are supported.

- Two version 1.2 DisplayPorts

  - ◼ Optional dithering or frame modulation from the 30-bpp internal display pipeline to 24- or 18-bit outputs on the DVI/HDMI/DisplayPort if not using a 30-bpp output mode.

## 2.5. DVI/HDMI Features

- Advanced DVI capability supporting 10-bit HDR (high dynamic range) output.

- Supports industry-standard CEA-861B video modes including 480p, 720p, 1080i, and 1080p. For a full list of currently supported modes, contact your local AMD support person.

- Maximum pixel rates for 24-bpp outputs are:

  - ◼ DVI—162 MP/s (megapixels per second) for single-link DVI

  - ◼ DVI—268.5 MP/s for dual-link DVI

  - ◼ HDMI—297 MP/s.

- Compliant with the DVI electrical specification.

- The HDMI specification meets the Windows Vista® logo requirements.

## 2.6. DisplayPort 1.2 Features

- Supports all the mandatory features of the *DisplayPort Standard Version 1.2* and the following optional features on links A, B, C, D, E, and F:
  - ACM packet-type support.
- ISRC packet-type support.
  - Each DisplayPort link can transport up to six video streams; one from each display engine.
  - Each DisplayPort link can support three options for the number of lanes and three options for link-data rate as follows:
- Four, two, or one lane(s).
- 5.4-, 2.7-, or 1.62-GHz link-data rate per lane.
- Supports all video modes supported by the display controller that do not oversubscribe the link bandwidth.
  - Examples of supported pixel-rate/resolution for four lanes at 5.4-GHz link rate:
    - Link bandwidth allows pixel clocks of up to 718 MP/s for 24 bpp or 574 MP/s for 30 bpp.
    - 2560 × 2048 @ 60Hz, 30 bpp is supported.
  - Examples of supported pixel-rate/resolution for two lanes at 5.4-GHz link rate:
    - Link bandwidth allows pixel clocks of up to 359 MP/s for 24 bpp or 287 MP/s for 30 bpp.
    - 2560 × 1600 @ 60Hz, 30 bpp is supported.
- Enhanced audio capabilities:
  - Supports PCM audio rates up to 192 kHz.
  - Dolby-TrueHD bit stream and DTS-HD Master Audio bit stream capable.

## 2.7. Integrated HD-Audio Controller (Azalia) and Codec

- HD-audio HDMI, DisplayPort, and wireless display outputs.
  - Multiple output stream DMAs.
  - Maximum output bandwidth of 73.728 Mbit/s.
  - Low power ECN support.
  - Hardware silent stream.
  - Function level reset.
  - Compatible Microsoft® UAA driver support for basic audio.
  - For advanced functionality (as follows), an AMD or a third party driver is required.
  - LPCM:
    - Speaker formats: 2.0, 2.1, 3.0, 4.0, 5.1, 6.1, and 7.1
    - Sample rates: 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz
    - Bits per sample: 16, 20, and 24
- Non-HBR Compressed audio pass-through up to 6.144 Mbps:

- **Supports AC-3, MPEG1, MP3 (MPEG1 layer 3), MPEG2, AAC, DTS, ATRAC, Dolby Digital+, WMA Pro, and DTS-HD.**
- HBR compressed audio pass-through up to 24.576 Mbps:
  - **Supports DTS-HD Master Audio and Dolby True HD.**
- Plug-and-Play:
  - **Sink audio format capabilities declaration.**
  - **Sink information.**
  - **AV association.**
- Lip sync information.
- HDCP content protection.

## 2.8. CRT DAC

- One integrated triple 10-bit DAC with built-in reference circuit, which takes output from either one of the internal display controllers (primary or secondary).
- A single RGB-CRT output.
- Support for the stereo-sync signal to drive a 3D display.
- A maximum pixel frequency of 400 MHz.
- An individual power-down feature for each of the three guns.
- Compliant with the VSIS electrical specification.
- Integrated with a built-in bandgap reference circuitry.
- A static detection circuitry (S_detect) for hot-plug/unplug capability.
- An integrated static monitor-detection circuit.

## 2.9. Bus Support Features

- Compliant with the PCI Express® Base Specification Revision 3.0, up to 8.0 GT/s.
- Fully inter-operative with PCI Express Base Specification Revision 2.1 and earlier devices.
- Supports ×1, ×2, ×4, ×8, and ×16 lane widths.
- Supports 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s link-data rates.
- Supports ×16 lane reversal where the receivers on lanes 0 to 15 on the graphics endpoint are mapped to the transmitters on lanes 15 down to 0 on the root complex.
- Supports ×16 lane reversal where the transmitters on lanes 0 to 15 on the graphics endpoint are mapped to the receivers on lanes 15 down to 0 on the root complex (requires corresponding support on the root complex).
- Supports full-swing and low-swing transmitter output levels.

# 3. PIN Assignment and Description

| Pin | Side B Connector | | Side A Connector | |
| --- | --- | --- | --- | --- |
| # | Name | Description | Name | Description |
| 1 | +12v | +12 volt power | PRSNT#1 | Hot plug presence detect |
| 2 | +12v | +12 volt power | +12v | +12 volt power |
| 3 | RSVD | Reserved | +12v | +12 volt power |
| 4 | GND | Ground | GND | Ground |
| 5 | SMCLK | SMBus clock | JTAG2 | TCK |
| 6 | SMDAT | SMBus data | JTAG3 | TDI |
| 7 | GND | Ground | JTAG4 | TDO |
| 8 | +3.3v | +3.3 volt power | JTAG5 | TMS |
| 9 | JTAG1 | +TRST# | +3.3v | +3.3 volt power |
| 10 | 3.3Vaux | 3.3v volt power | +3.3v | +3.3 volt power |
| 11 | WAKE# | Link Reactivation | PWRGD | Power Good |
| **Mechanical Key** | | | | |
| 12 | RSVD | Reserved | GND | Ground |
| 13 | GND | Ground | REFCLK+ | Reference Clock |
| 14 | HSOp(0) | Transmitter Lane 0, | REFCLK- | Differential pair |
| 15 | HSOn(0) | Differential pair | GND | Ground |
| 16 | GND | Ground | HSIp(0) | Receiver Lane 0, |
| 17 | PRSNT#2 | Hotplug detect | HSIn(0) | Differential pair |
| 18 | GND | Ground | GND | Ground |
| 19 | HSOp(1) | Transmitter Lane 1, | RSVD | Reserved |
| 20 | HSOn(1) | Differential pair | GND | Ground |
| 21 | GND | Ground | HSIp(1) | Receiver Lane 1, |
| 22 | GND | Ground | HSIn(1) | Differential pair |
| 23 | HSOp(2) | Transmitter Lane 2, | GND | Ground |

| Pin | Side B Connector | | Side A Connector | |
|---|---|---|---|---|
| # | Name | Description | Name | Description |
| 24 | HSOn(2) | Differential pair | GND | Ground |
| 25 | GND | Ground | HSIp(2) | Receiver Lane 2, Differential pair |
| 26 | GND | Ground | HSIn(2) | |
| 27 | HSOp(3) | Transmitter Lane 3, Differential pair | GND | Ground |
| 28 | HSOn(3) | | GND | Ground |
| 29 | GND | Ground | HSIp(3) | Receiver Lane 3, Differential pair |
| 30 | RSVD | Reserved | HSIn(3) | |
| 31 | PRSNT#2 | Hot plug detect | GND | Ground |
| 32 | GND | Ground | RSVD | Reserved |
| 33 | HSOp(4) | Transmitter Lane 4, Differential pair | RSVD | Reserved |
| 34 | HSOn(4) | | GND | Ground |
| 35 | GND | Ground | HSIp(4) | Receiver Lane 4, Differential pair |
| 36 | GND | Ground | HSIn(4) | |
| 37 | HSOp(5) | Transmitter Lane 5, Differential pair | GND | Ground |
| 38 | HSOn(5) | | GND | Ground |
| 39 | GND | Ground | HSIp(5) | Receiver Lane 5, Differential pair |
| 40 | GND | Ground | HSIn(5) | |
| 41 | HSOp(6) | Transmitter Lane 6, Differential pair | GND | Ground |
| 42 | HSOn(6) | | GND | Ground |
| 43 | GND | Ground | HSIp(6) | Receiver Lane 6, Differential pair |
| 44 | GND | Ground | HSIn(6) | |
| 45 | HSOp(7) | Transmitter Lane 7, Differential pair | GND | Ground |
| 46 | HSOn(7) | | GND | Ground |
| 47 | GND | Ground | HSIp(7) | Receiver Lane 7, Differential pair |
| 48 | PRSNT#2 | Hot plug detect | HSIn(7) | |
| 49 | GND | Ground | GND | Ground |
| 50 | HSOp(8) | Transmitter Lane 8, | RSVD | Reserved |

| Pin | Side B Connector | | Side A Connector | |
|---|---|---|---|---|
| # | Name | Description | Name | Description |
| 51 | HSOn(8) | Differential pair | GND | Ground |
| 52 | GND | Ground | HSIp(8) | Receiver Lane 8, Differential pair |
| 53 | GND | Ground | HSIn(8) | |
| 54 | HSOp(9) | Transmitter Lane 9, Differential pair | GND | Ground |
| 55 | HSOn(9) | | GND | Ground |
| 56 | GND | Ground | HSIp(9) | Receiver Lane 9, Differential pair |
| 57 | GND | Ground | HSIn(9) | |
| 58 | HSOp(10) | Transmitter Lane 10, Differential pair | GND | Ground |
| 59 | HSOn(10) | | GND | Ground |
| 60 | GND | Ground | HSIp(10) | Receiver Lane 10, Differential pair |
| 61 | GND | Ground | HSIn(10) | |
| 62 | HSOp(11) | Transmitter Lane 11, Differential pair | GND | Ground |
| 63 | HSOn(11) | | GND | Ground |
| 64 | GND | Ground | HSIp(11) | Receiver Lane 11, Differential pair |
| 65 | GND | Ground | HSIn(11) | |
| 66 | HSOp(12) | Transmitter Lane 12, Differential pair | GND | Ground |
| 67 | HSOn(12) | | GND | Ground |
| 68 | GND | Ground | HSIp(12) | Receiver Lane 12, Differential pair |
| 69 | GND | Ground | HSIn(12) | |
| 70 | HSOp(13) | Transmitter Lane 13, Differential pair | GND | Ground |
| 71 | HSOn(13) | | GND | Ground |
| 72 | GND | Ground | HSIp(13) | Receiver Lane 13, Differential pair |
| 73 | GND | Ground | HSIn(13) | |
| 74 | HSOp(14) | Transmitter Lane 14, Differential pair | GND | Ground |
| 75 | HSOn(14) | | GND | Ground |
| 76 | GND | Ground | HSIp(14) | Receiver Lane 14, Differential pair |
| 77 | GND | Ground | HSIn(14) | |

| Pin | Side B Connector | | Side A Connector | |
|---|---|---|---|---|
| # | Name | Description | Name | Description |
| 78 | HSOp(15) | Transmitter Lane 15, Differential pair | GND | Ground |
| 79 | HSOn(15) | | GND | Ground |
| 80 | GND | Ground | HSIp(15) | Receiver Lane 15, Differential pair |
| 81 | PRSNT#2 | Hot plug present detect | HSIn(15) | |
| 82 | RSVD#2 | Hot Plug Detect | GND | Ground |

# 4. Power Consumption

| Application | Total ASIC Power + DRAM Power (W) |
|---|---|
| Static Windows - 65c | **6.72** |

| Application | Total ASIC Power + DRAM Power (W) |
|---|---|
| 3D Mark Vantage FT6 | **30.63** |

# 5. Board Dimension

## 5.1 Board Dimension

**(Unit : mm)**



145mm

111mm
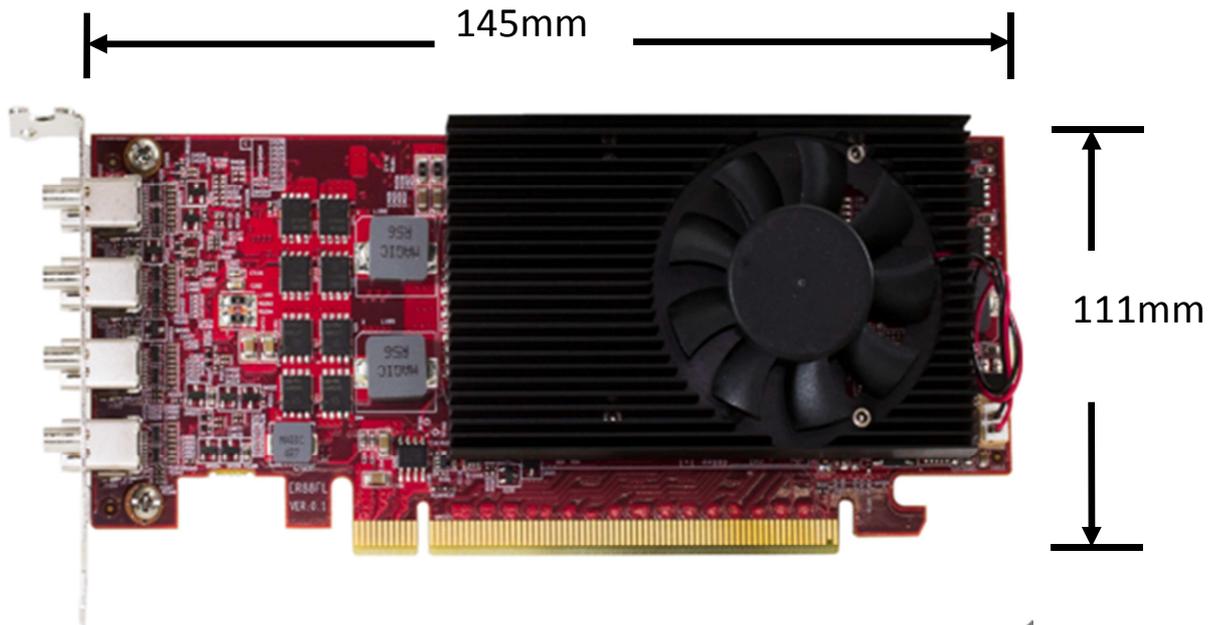
**Tolerances: +/_ 0.13 mm**

# 6. <u>Thermal Mechanism</u>

## 6.1. Fan-Sink Thermal Module
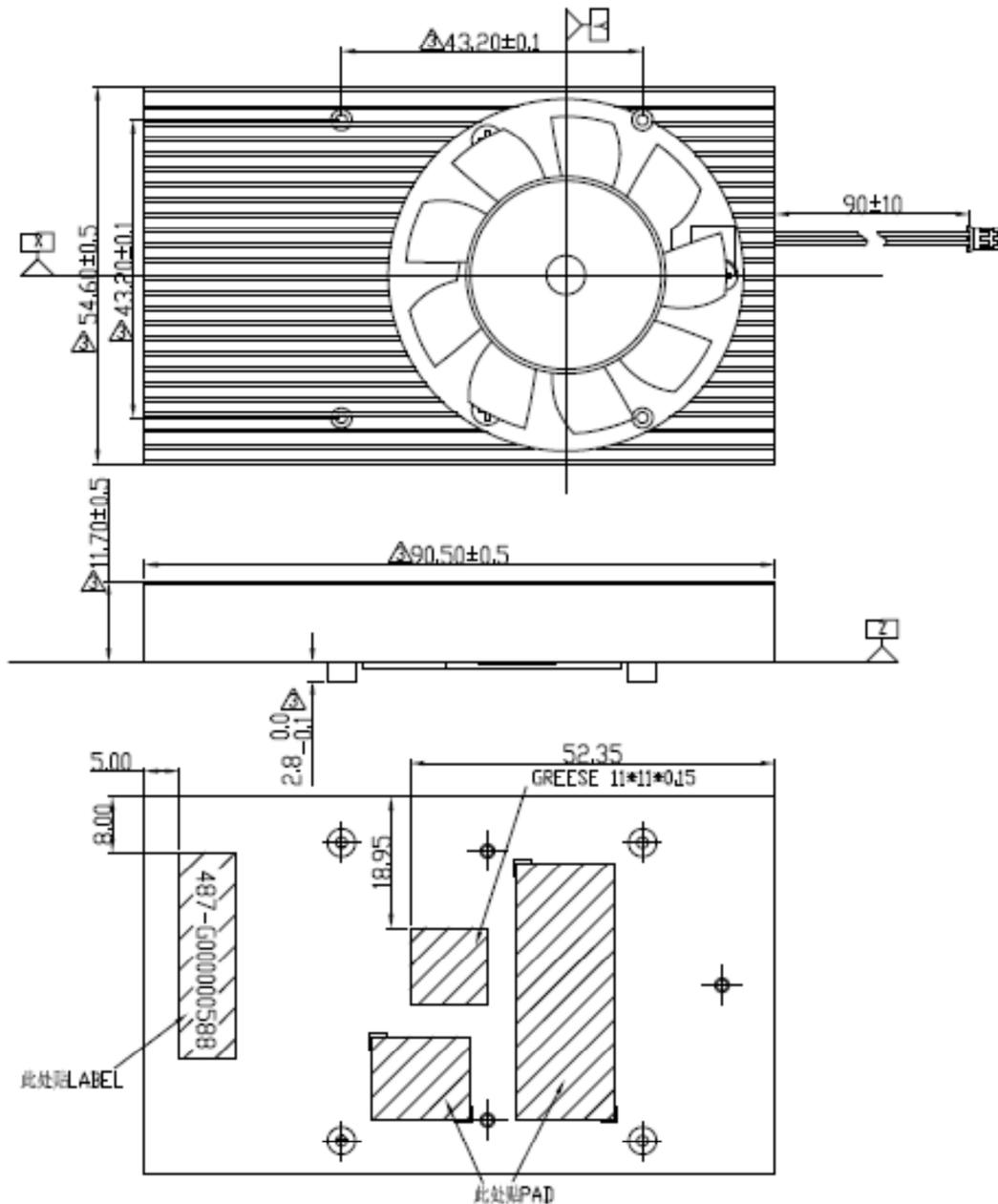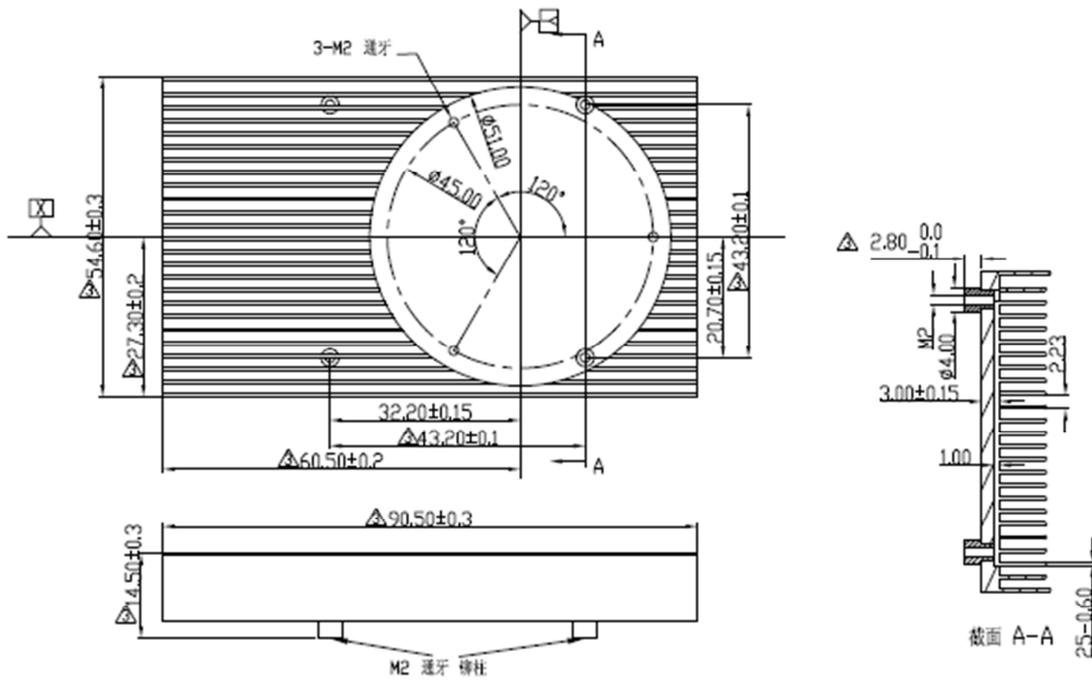
| Tolerances | |
|---|---|
| 0-10 | +/- 0.1 |
| 10-50 | +/- 0.15 |
| 50-100 | +/- 0.2 |
| 100~ | +/- 0.25 |

# Change log or update history

| Rev. | Date | Description |
|------|------|-------------|
| 0.1 | 2014/3/27 | 1$^{st}$ Draft. |
| | | |