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Apacer Technology Inc.

CUSTOMER: 研華股份有限公司

APPROVAL SHEET

APPROVED NO.	**:**	**90004-T0019**
ISSUE DATE	**:**	**July-12-2012**
MODULE PART NO.	**:**	**78.A1GE3.AFF0C**
PCB PART NO.	**:**	**48.18213.09F0C**
IC Brand	**:**	**Hynix**
DESCRIPTION	**:**	**DDR3 DIMM 12800-11 256x8 2GB HYN VLP G**

CUSTOMER APPROVAL :

Apacer Technology Inc.

Authorized by : Steven Wang

2GB Unbuffered VLP DDR3 SDRAM DIMM with SPD

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency	Density	Organization	Component Composition	Number of Rank
78.A1GE3.AFF0C	12.8GB/sec	1600Mbps	800MHz	CL11	2GB	256Mx64	256Mx8*8EA	1

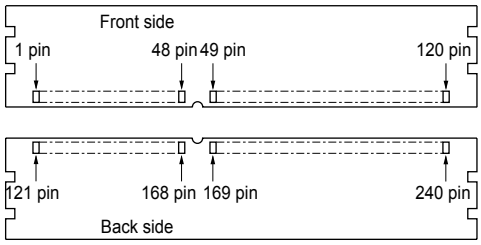
Specifications

- On Dimm Thermal Sensor: No
- Density: 2GB
- Organization
  - 256M words × 64 bits, 1 rank
- Mounting 8 pieces of 2G bits DDR3 SDRAM sealed in FBGA
- Package: 240-pin socket type dual in line memory module (DIMM)
  - PCB height: 18.75mm
  - Lead pitch: 1.0mm (pin)
  - Lead-free (RoHS compliant)
- Power supply: VDD = 1.5V ± 0.075V
- Eight internal banks for concurrent operation (components)
- Interface: SSTL_15
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- /CAS Latency (CL): 6, 7, 8, 9, 10, 11
- /CAS write latency (CWL): 5, 6, 7
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles
  - Average refresh period
    7.8μs at 0°C ≤ TC ≤ +85°C
    3.9μs at +85°C < TC ≤ +95°C
- Operating case temperature range
  - TC = 0°C to +95°C

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die-Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for temperature read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function
- SRT range:
  - Normal/extended
  - Auto/manual self-refresh
- Programmable Output driver impedance control

Pin Configurations



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREFDQ	61	A2	121	VSS	181	A1
2	VSS	62	VDD	122	DQ4	182	VDD
3	DQ0	63	NC	123	DQ5	183	VDD
4	DQ1	64	NC	124	VSS	184	CK0
5	VSS	65	VDD	125	DM0	185	/CK0
6	/DQS0	66	VDD	126	NC	186	VDD
7	DQS0	67	VREFCA	127	VSS	187	NC
8	VSS	68	NC	128	DQ6	188	A0
9	DQ2	69	VDD	129	DQ7	189	VDD
10	DQ3	70	A10(AP)	130	VSS	190	BA1
11	VSS	71	BA0	131	DQ12	191	VDD
12	DQ8	72	VDD	132	DQ13	192	/RAS
13	DQ9	73	/WE	133	VSS	193	/CS0
14	VSS	74	/CAS	134	DM1	194	VDD
15	/DQS1	75	VDD	135	NC	195	ODT0
16	DQS1	76	NC	136	VSS	196	A13
17	VSS	77	NC	137	DQ14	197	VDD
18	DQ10	78	VDD	138	DQ15	198	NC
19	DQ11	79	NC	139	VSS	199	VSS
20	VSS	80	VSS	140	DQ20	200	DQ36
21	DQ16	81	DQ32	141	DQ21	201	DQ37
22	DQ17	82	DQ33	142	VSS	202	VSS
23	VSS	83	VSS	143	DM2	203	DM4
24	/DQS2	84	/DQS4	144	NC	204	NC
25	DQS2	85	DQS4	145	VSS	205	VSS
26	VSS	86	VSS	146	DQ22	206	DQ38
27	DQ18	87	DQ34	147	DQ23	207	DQ39
28	DQ19	88	DQ35	148	VSS	208	VSS
29	VSS	89	VSS	149	DQ28	209	DQ44
30	DQ24	90	DQ40	150	DQ29	210	DQ45
31	DQ25	91	DQ41	151	VSS	211	VSS
32	VSS	92	VSS	152	DM3	212	DM5
33	/DQS3	93	/DQS5	153	NC	213	NC
34	DQS3	94	DQS5	154	VSS	214	VSS
35	VSS	95	VSS	155	DQ30	215	DQ46
36	DQ26	96	DQ42	156	DQ31	216	DQ47

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
37	DQ27	97	DQ43	157	VSS	217	VSS
38	VSS	98	VSS	158	NC	218	DQ52
39	NC	99	DQ48	159	NC	219	DQ53
40	NC	100	DQ49	160	VSS	220	VSS
41	VSS	101	VSS	161	NC	221	DM6
42	NC	102	/DQS6	162	NC	222	NC
43	NC	103	DQS6	163	VSS	223	VSS
44	VSS	104	VSS	164	NC	224	DQ54
45	NC	105	DQ50	165	NC	225	DQ55
46	NC	106	DQ51	166	VSS	226	VSS
47	VSS	107	VSS	167	NC	227	DQ60
48	NC	108	DQ56	168	/RESET	228	DQ61
49	NC	109	DQ57	169	NC	229	VSS
50	CKE0	110	VSS	170	VDD	230	DM7
51	VDD	111	/DQS7	171	A15/NC*	231	NC
52	BA2	112	DQS7	172	A14/NC*	232	VSS
53	NC	113	VSS	173	VDD	233	DQ62
54	VDD	114	DQ58	174	A12	234	DQ63
55	A11	115	DQ59	175	A9	235	VSS
56	A7	116	VSS	176	VDD	236	VDDSPD
57	VDD	117	SA0	177	A8	237	SA1
58	A5	118	SCL	178	A6	238	SDA
59	A4	119	SA2	179	VDD	239	VSS
60	VDD	120	VTT	180	A3	240	VTT

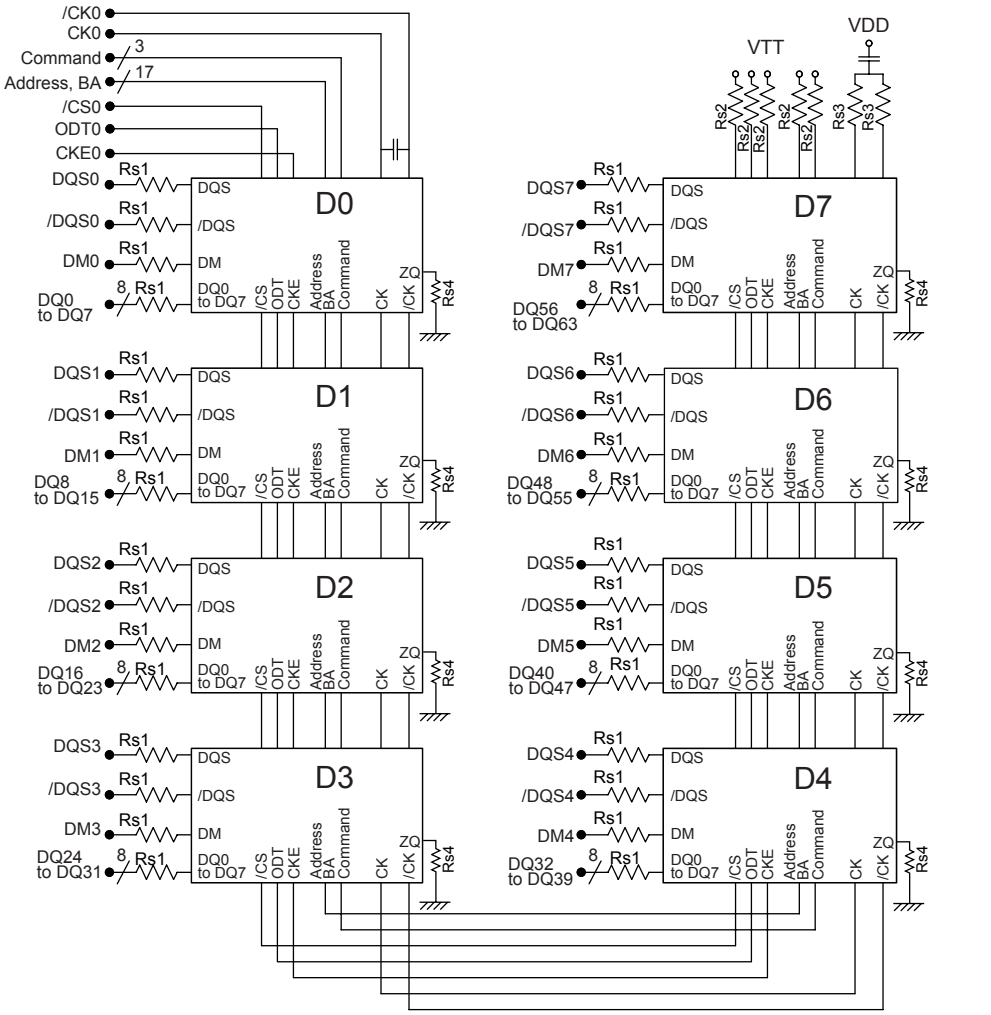
*IC Componet Composition :

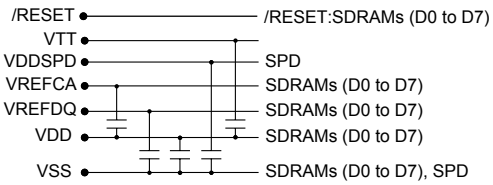
256Mx8 A0~A14
512Mx8 A0~A15
1024Mx8 A0~A15

Pin Description

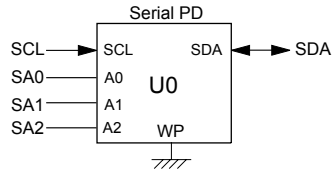
Pin name	Function
A0 to A14	Address input Row address A0 to A14 Column address A0 to A9
A10 (AP)	Auto precharge
A12 (/BC)	Burst chop
BA0, BA1, BA2	Bank select address
DQ0 to DQ63	Data input/output
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
/CS0	Chip select
CKE0	Clock enable
CK0	Clock input
/CK0	Differential clock input
DQS0 to DQS7, /DQS0 to /DQS7	Input and output data strobe
DM0 to DM7	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SA0, SA1, SA2	Serial address input
VDD	Power for internal circuit
VDDSPD	Power for serial EEPROM
VREFCA	Reference voltage for CA
VREFDQ	Reference voltage for DQ
VSS	Ground
VTT	I/O termination supply for SDRAM
/RESET	Set DRAM to known state
ODT0	ODT control
NC	No connection

Block Diagram

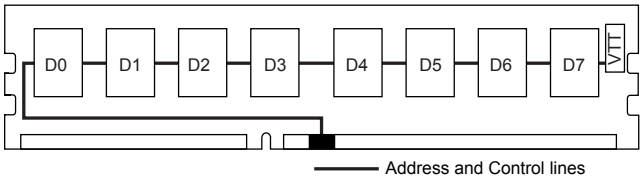




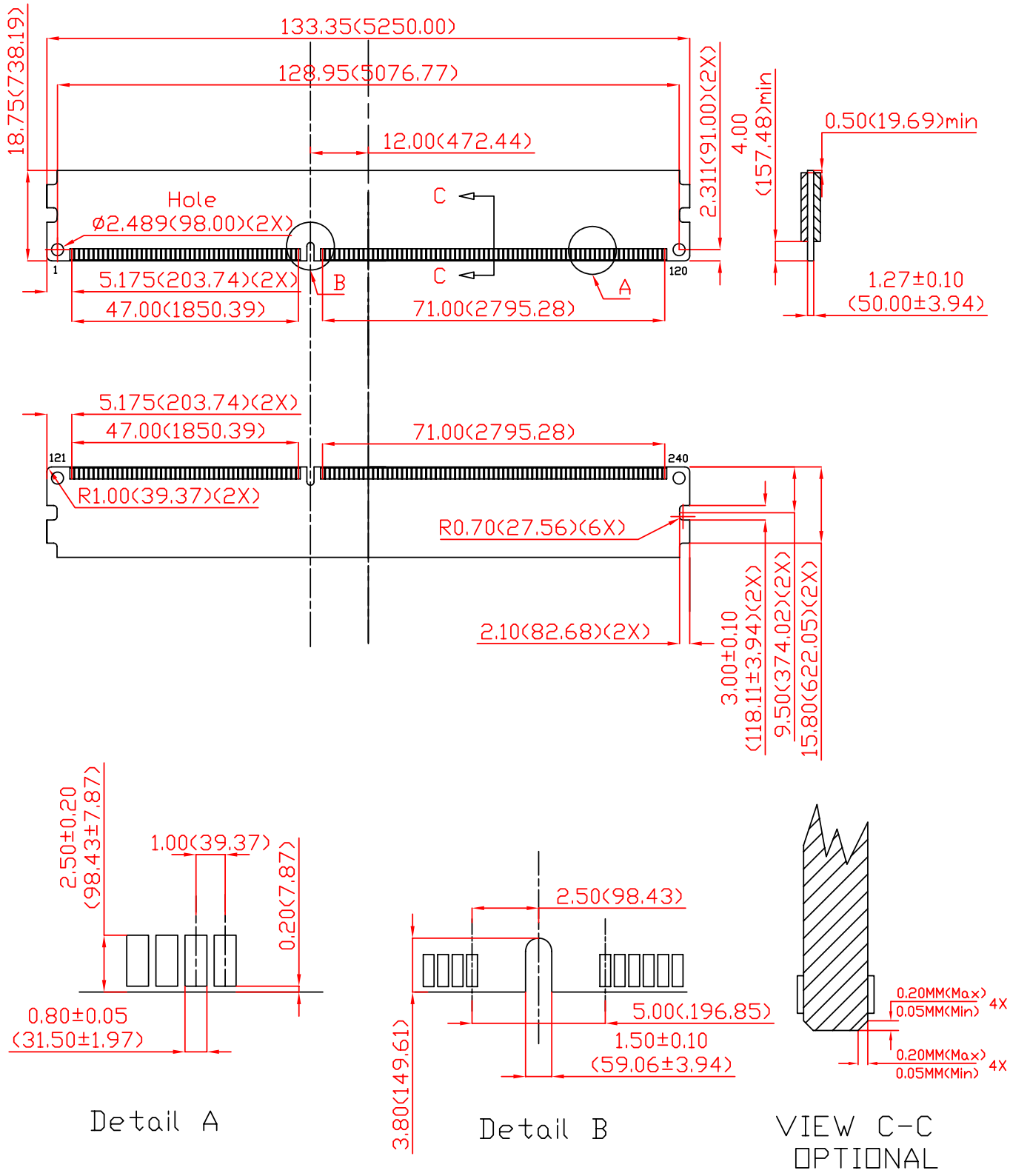
Notes :
1. DQ wiring may be changed within a byte.
2. DQ, DQS, /DQS, ODT, DM, CKE, /CS relationships must be maintained as shown.



* D0 to D7: 2G bits DDR3 SDRAM
Address, BA: A0 to A14, BA0 to BA2
Command: /RAS, /CAS, /WE
U0: 256 bytes EEPROM
Rs1: 15Ω
Rs2: 39Ω
Rs3: 36Ω
Rs4: 240Ω



Physical Outline



(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)